

BOM Groups

BOM GROUP	BOM OPTIONS
J44_COMMON	ALTERNATE,COMMON,J44_COMMON1,J44_COMMON2,J44_COMMON3,J44_COMMON4,J44_PROGPARTS
J44_COMMON1	TBTHV:P15V,SKIP_5V3V3:AUDIBLE,SPI:DUAL_IO
J44_COMMON2	EDP,EDP_LS_CAP,CAMERA_3V3:S0,CAM_WAKE:NO,CAM_XTAL:NO,MEM_ODT:PU,VCORE_FETS
J44_COMMON3	XDP,LPCPLUS,BKLT:PROD,CPU_THRM:ALRT,LOADRC:NO,OTHERRC:NO,DDRRC:NO,TBTRC:NO,BMONRC:NO
J44_PROGPARTS	SMC_PROG:PVT,BOOTROM:PVT,TBTROM:PVT,TPAD_PSOC:PROG
ENGISNS	LOADISNS,OTHERISNS,DDRISNS,TBTISNS,BMONISNS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4596	1	HSWULT,SR18A,PRQ,C0,2,4,28W,2+3,3M,BGA	U0500	CRITICAL	CPU_HSW:2.4G
337S4597	1	HSWULT,SR189,PRQ,C0,2,6,28W,2+3,3M,BGA	U0500	CRITICAL	CPU_HSW:2.6G
337S4598	1	HSWULT,SR188,PRQ,C0,2,8,28W,2+3,4M,BGA	U0500	CRITICAL	CPU_HSW:2.8G
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR13C,FCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
376S0964	2	MOSFET,N-CH,25V,30A,9.6M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET,N-CH,25V,30A,6.1M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN

Programmables (All Builds)

TBT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3918	1	EPROM,FALCON RIDGE (V13.7) J44	U2890	CRITICAL	TBTROM:PVT

SMC

341S3922	1	IC,SMC-B1,EXT(V2.16F39),PVT,J44	U5000	CRITICAL	SMC_PROG:PVT
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EFI ROM

341S3924	1	IC,EFI ROM (V0116),PVT,J44	U6100	CRITICAL	BOOTROM:PVT
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PSOC

341S3862	1	IC,TRKPD/KYBD PSOC,CU ONLY(V224) J44	U4801	CRITICAL	TPAD_PSOC:PROG
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Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	
128S0311	128S0329		ALL	
138S0739	138S0706		ALL	
197S0481	197S0480		ALL	
152S0461	152S1645		ALL	
376S1080	376S0820		ALL	
155S0667	155S0583		ALL	
138S0725	138S0724		ALL	
376S1032	376S0855		ALL	
376S1129	376S0855		ALL	
376S1089	376S1128		ALL	
353S3452	353S1286		ALL	
376S1180	376S0761		ALL	
128S0364	128S0264		ALL	
107S0254	107S0241		ALL	
138S0843	138S0674		ALL	
138S0803	138S0639		ALL	
138S0846	138S0811		ALL	
197S0542	197S0544		ALL	
197S0545	197S0544		ALL	
152S1876	152S1804		ALL	
107S0255	107S0240		ALL	
107S0250	107S0248		ALL	
127S0164	127S0162		ALL	
353S4070	353S4069		ALL	
353S4068	353S4069		ALL	
353S3814	353S3812		ALL	
311S0649	311S0541		ALL	
128S0436	128S0392		ALL	

Diodes alt to Fairchild
NEC alt to Sanyo
Samsung alt to Murata
Epson alt to NDK
Cyntec alt to Vishay
Diodes alt to On Semi
Panasonic alt to TDK
Samsung alt to Murata
Toshiba alt for Diodes Dual
NXP Alt for Diodes Dual
NXP Alt for Diodes Single
Maxim alt to Microchip
Renesas alt to Vishay
Sanyo 2nd Factory alt
Cyntec alt to TFT
Samsung alt to Murata (BKLT)
Samsung alt to Murata (BKLT)
Samsung alt to Murata (BKLT)
NDK alt to TXC
Epson alt to TXC
TDK alt to Toko
Cyntec alt to TFT
Cyntec alt to TFT
Rohm alt to Vishay
Pericom alt to TI DP Mux U9750
NXP alt to TI DP Mux U9750
TI alt to NXP
ONsemi alt to Toshiba
Kemet alt to Sanyo

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BOM Configuration											
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0054	COMMON,MLB-4GB,J44	J44_COMMON
985-0053	DEV,MLB-4GB,J44	XDP_CONN
639-4878	PCBA,MLB-4GB,2.4G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-4879	PCBA,MLB-4GB,2.4G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G_ELPIDA,CAMDRAM:ELPIDA
639-4880	PCBA,MLB-4GB,2.4G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.4G,RAM_4G_MICRON,CAMDRAM:MICRON
639-5272	PCBA,MLB-4GB,2.6G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-5273	PCBA,MLB-4GB,2.6G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G_ELPIDA,CAMDRAM:ELPIDA
639-5274	PCBA,MLB-4GB,2.6G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.6G,RAM_4G_MICRON,CAMDRAM:MICRON
639-5275	PCBA,MLB-4GB,2.8G,4GB-HYNIX,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G_HYNIX_H,CAMDRAM:HYNIX_H
639-5276	PCBA,MLB-4GB,2.8G,4GB-ELPIDA,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G_ELPIDA,CAMDRAM:ELPIDA
639-5277	PCBA,MLB-4GB,2.8G,4GB-MICRON,J44	BASE_BOM,CPU_HSW:2.8G,RAM_4G_MICRON,CAMDRAM:MICRON
685-0074	VCORE,FET,VSHY,J44	VCORE_FET:VSHY
685-0075	VCORE,FET,REN,J44	VCORE_FET:REN

DEVELOPMENT/BASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0054	1	J44 MLB COMMON BOM	BASE	CRITICAL	BASE_BOM
985-0053	1	J44 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SUB-BOMS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0074	1	VCORE,FET,VSHY,J44	VCOREFETS	CRITICAL	VCORE_FETS

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0075	685-0074		ALL	REPLACE ALT TO VISHAY

DRAM PARTS

333S0704	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,F,DIE,96FBGA	00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000	CRITICAL	4G_ELPIDA
333S0700	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,HUMA,96FBGA	00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000	CRITICAL	4G_HYNIX_H
333S0698	8	1C,SDRAM,4GBIT,256MX16,DDR3-1600,REV E,96FBGA	00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000	CRITICAL	4G_MICRON
333S0715	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,F,DIE,96FBGA	00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000	CRITICAL	4G_ELPIDA_1866
333S0717	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,HUMA,96FBGA	00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000	CRITICAL	4G_HYNIX_H_1866
333S0720	8	1C,SDRAM,4GBIT,256MX16,DDR3-1866,REV E,96FBGA	00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000,00000	CRITICAL	4G_MICRON_1866

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_4G_ELPIDA	4G_ELPIDA,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L,PPDDR:1V35
RAM_4G_HYNIX_H	4G_HYNIX_H,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H,PPDDR:1V35
RAM_4G_MICRON	4G_MICRON,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L,PPDDR:1V35
RAM_4G_ELPIDA_1866	4G_ELPIDA_1866,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L,PPDDR:1V5
RAM_4G_HYNIX_H_1866	4G_HYNIX_H_1866,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H,PPDDR:1V5
RAM_4G_MICRON_1866	4G_MICRON_1866,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L,PPDDR:1V5

NOTE: 1866 PARTS BEING STRAPPED TO RUN AT 1600

13" MBP VARIABLE BOM GROUPS

BOM GROUP	BOM OPTIONS
J44_COMMON4	SMCBOARDID:8

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
CAMDRAM:HYNIX_H	CAMDRAM_TYPE:HYNIX_H
CAMDRAM:ELPIDA	CAMDRAM_TYPE:ELPIDA
CAMDRAM:MICRON	CAMDRAM_TYPE:MICRON

DRAM Parts


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0700	1	1C,SDRAM,4GBIT,DDR3L-1600,HUMA,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:HYNIX_H
333S0704	1	1C,SDRAM,4GBIT,DDR3L-1600,DIE P,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:ELPIDA
333S0698	1	1C,SDRAM,4GBIT,DDR3L-1600,REV E,96B FBGA	U4000	CRITICAL	CAMDRAM_TYPE:MICRON

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BOM Configuration

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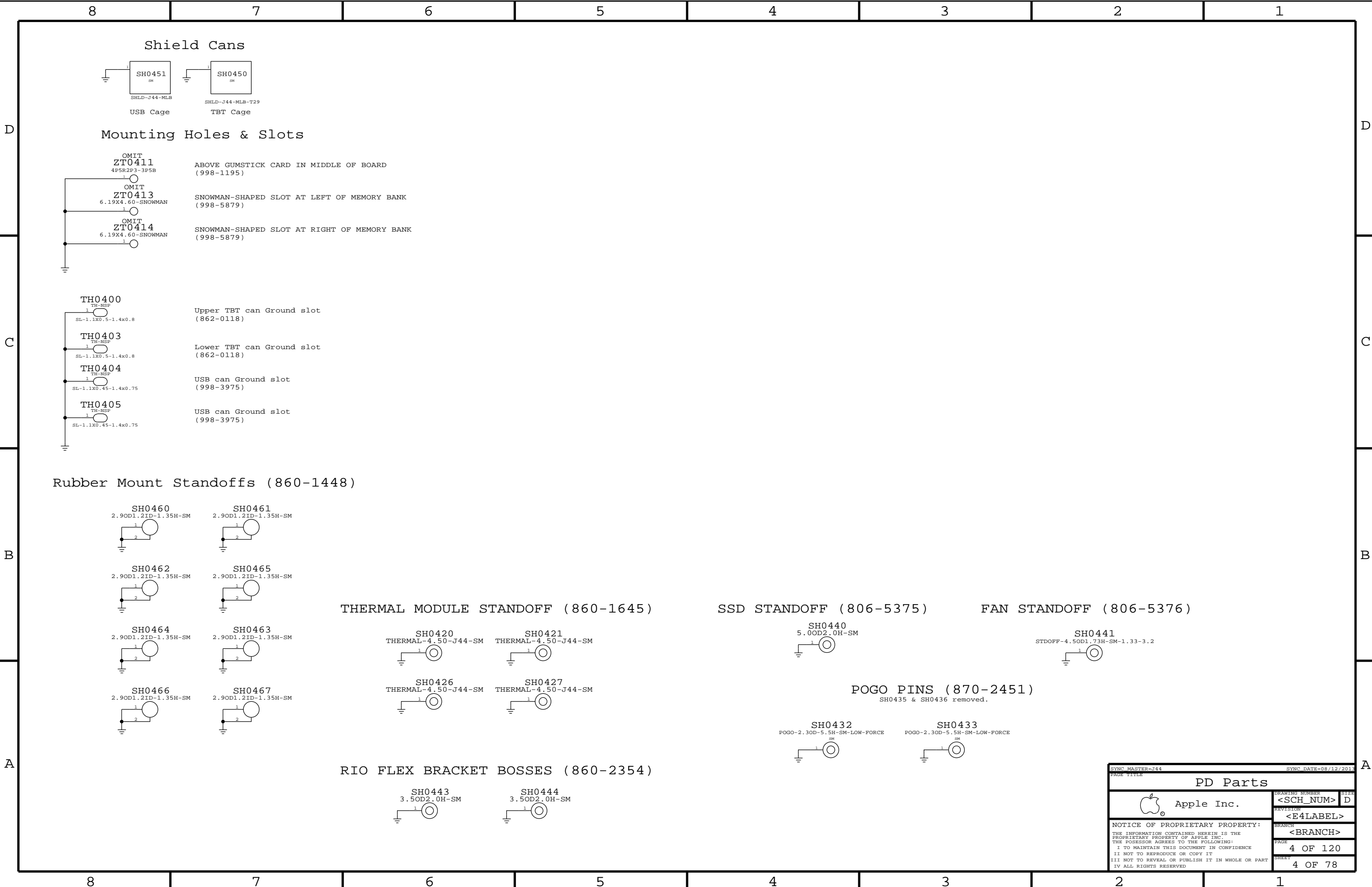
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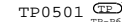
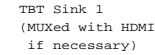
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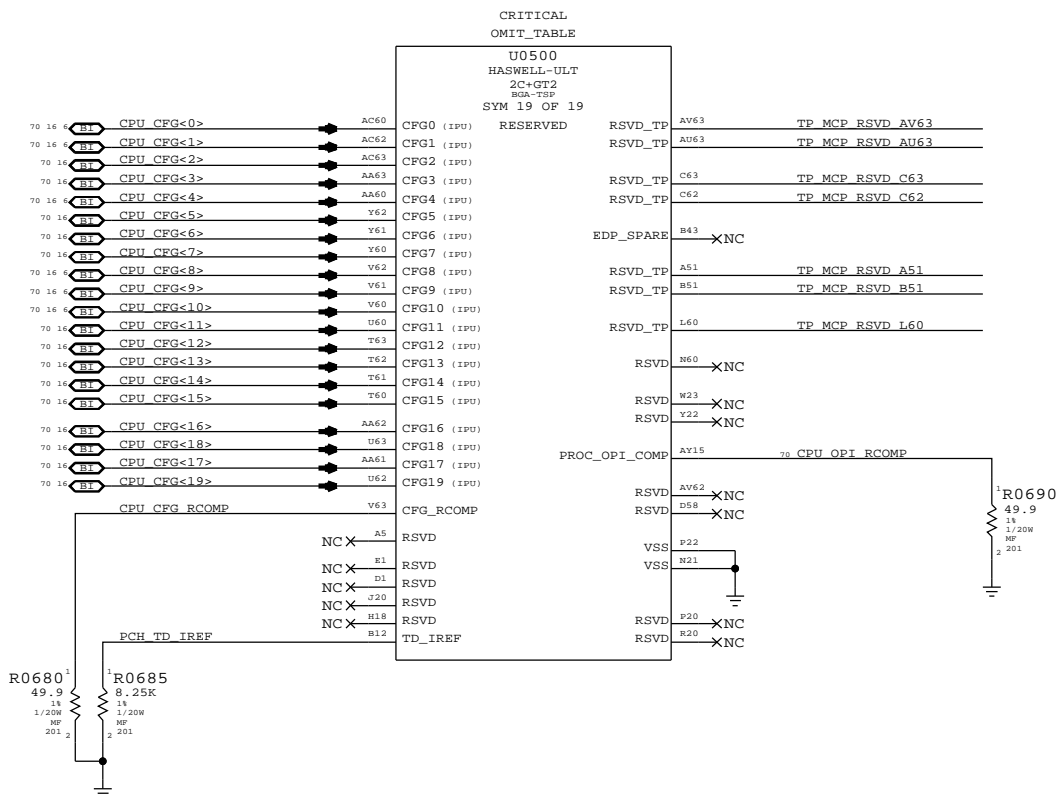
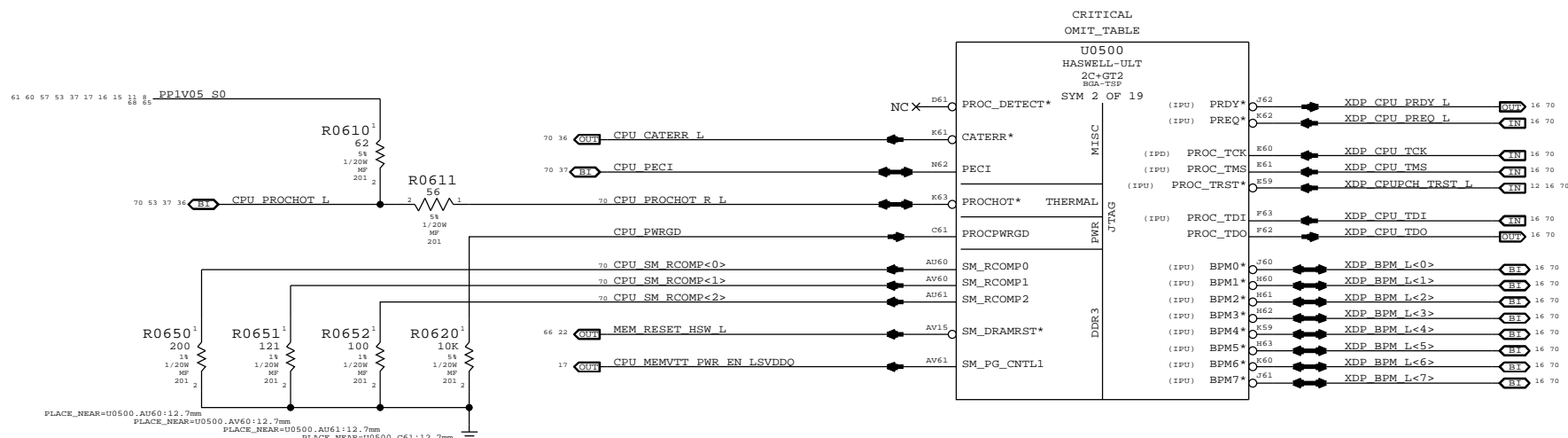
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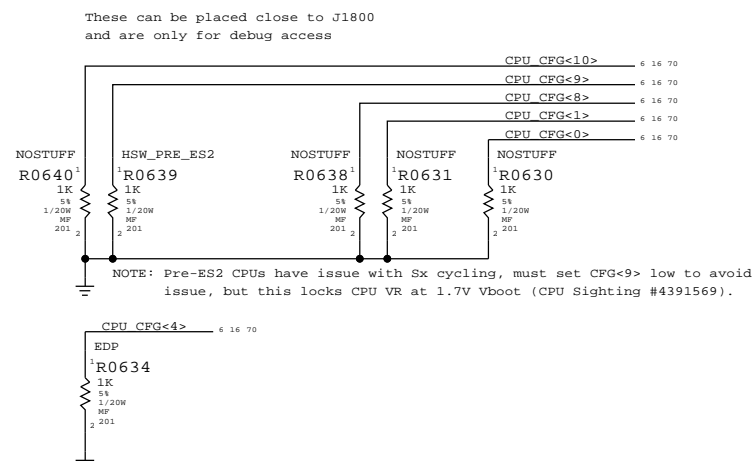



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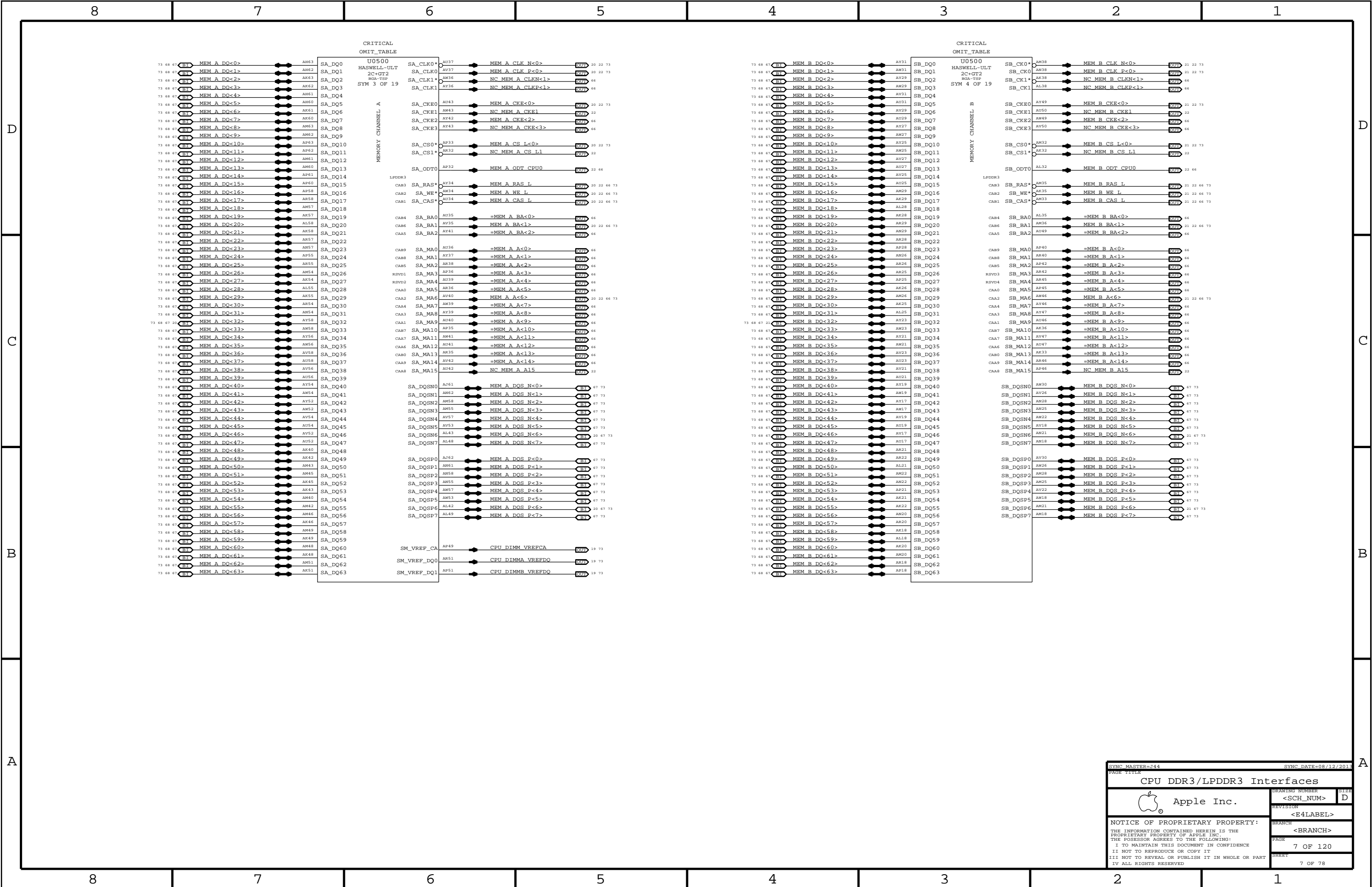


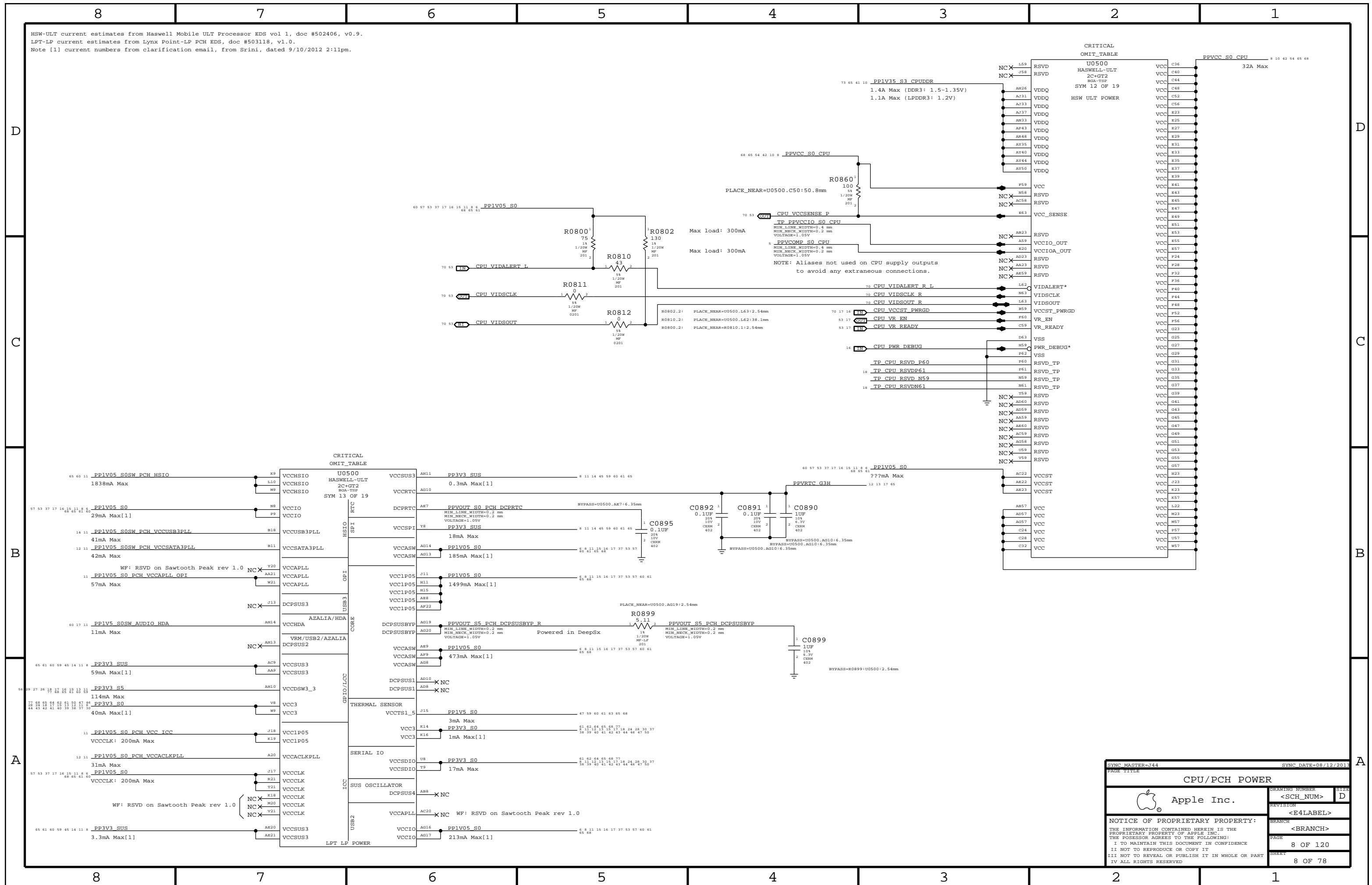


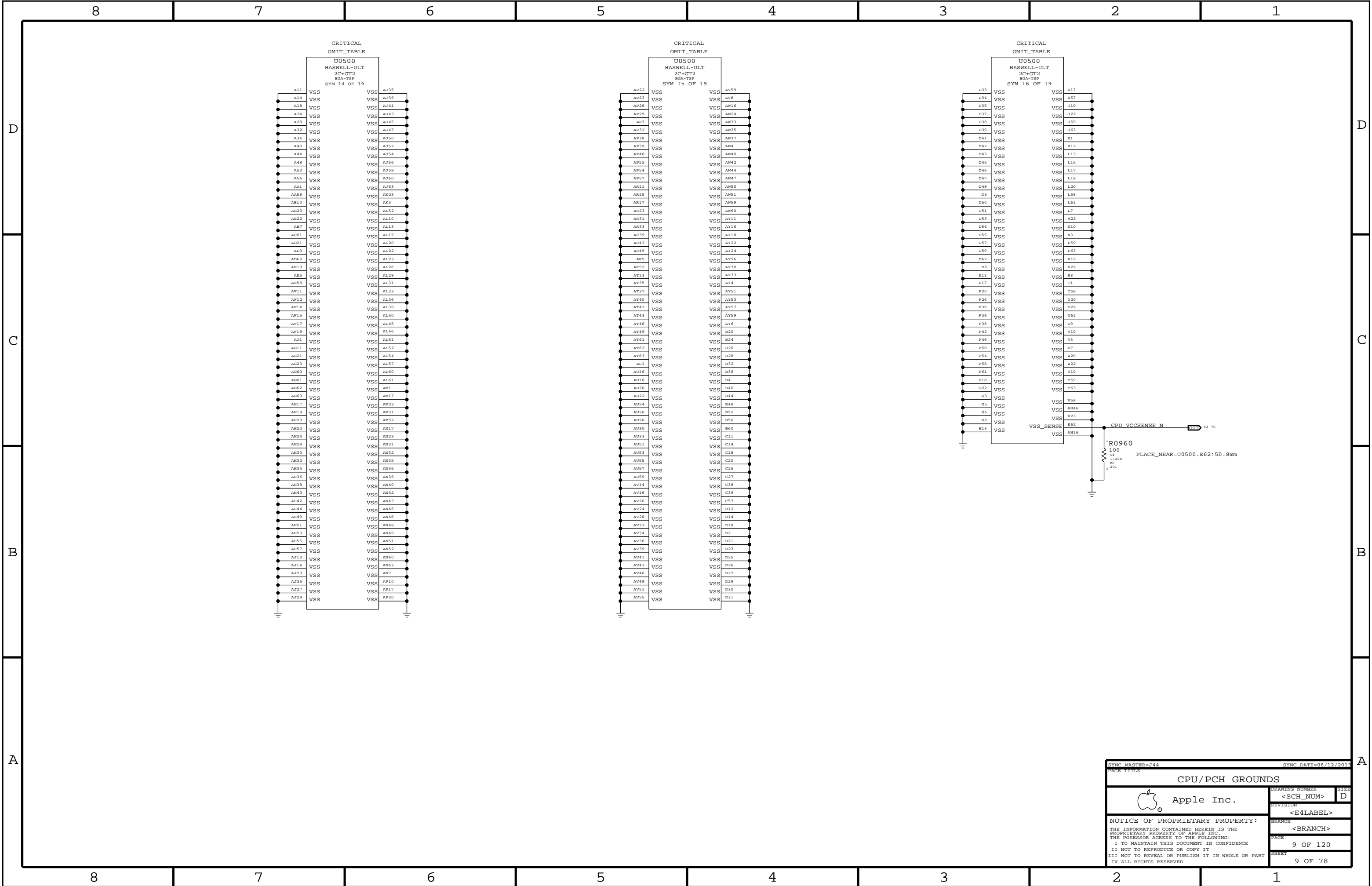
CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9>:NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8>:ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4>:eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1>:PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0>:RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

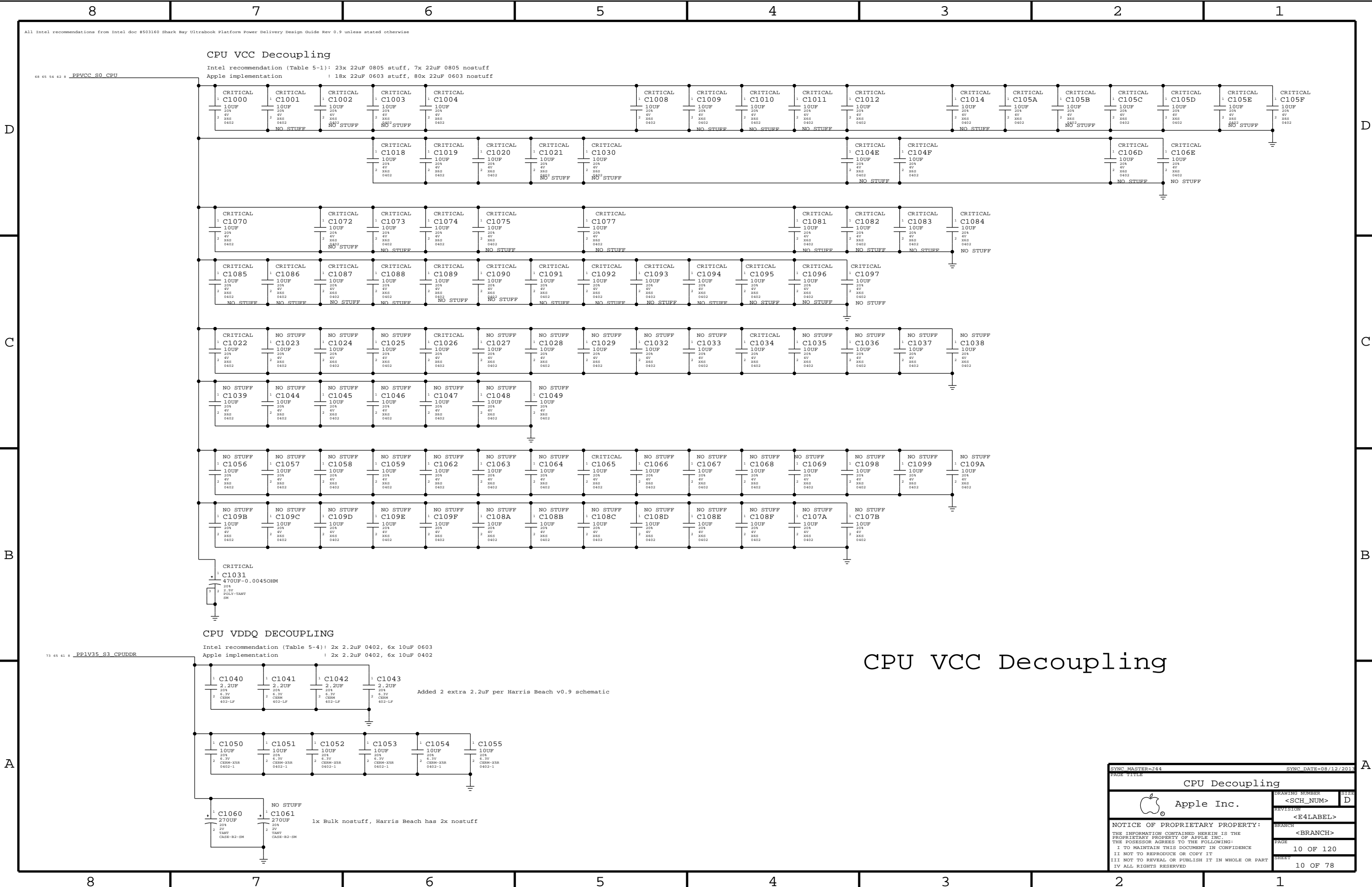


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CPU Misc/JTAG/CFG/RSVD			
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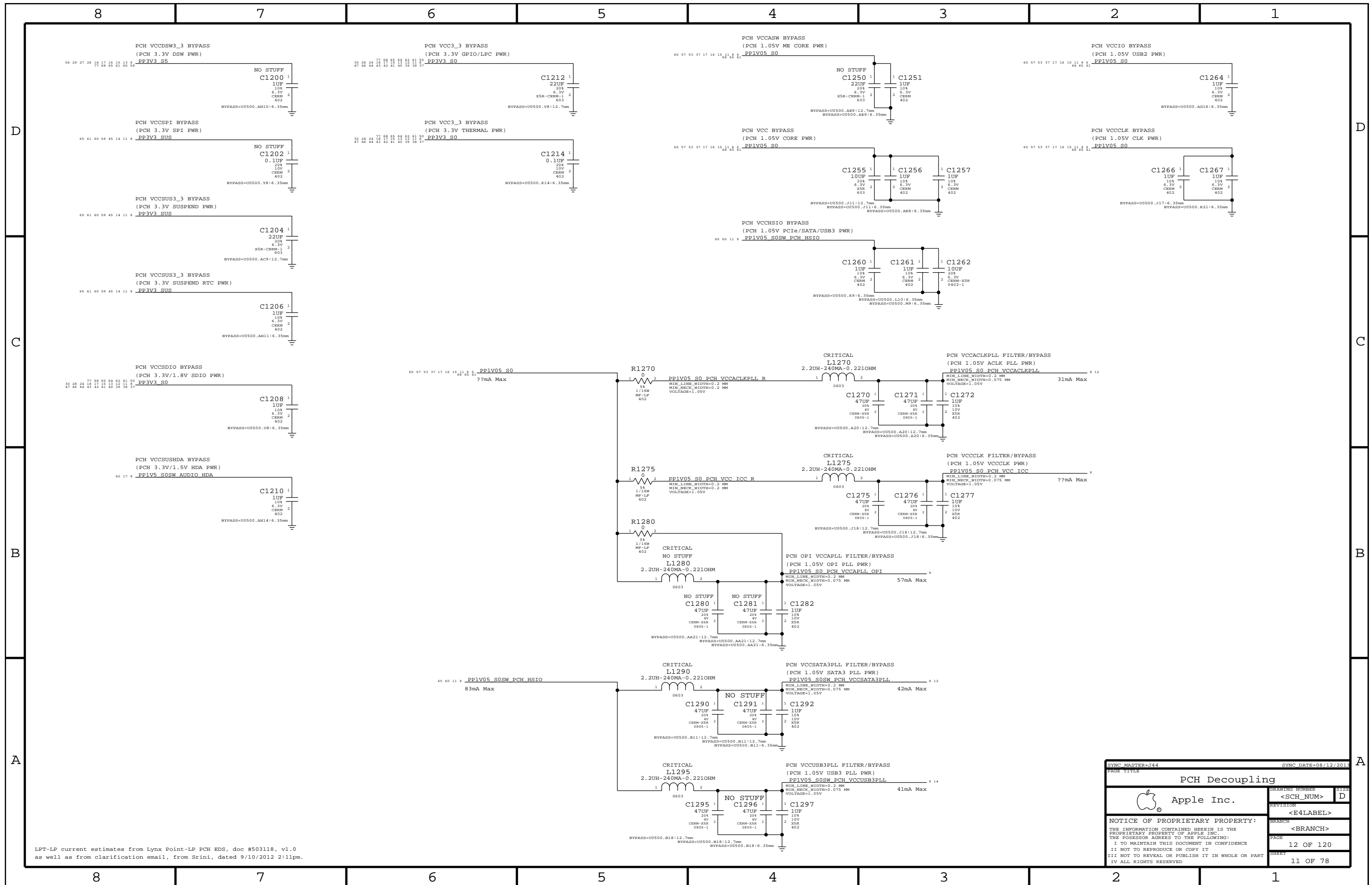


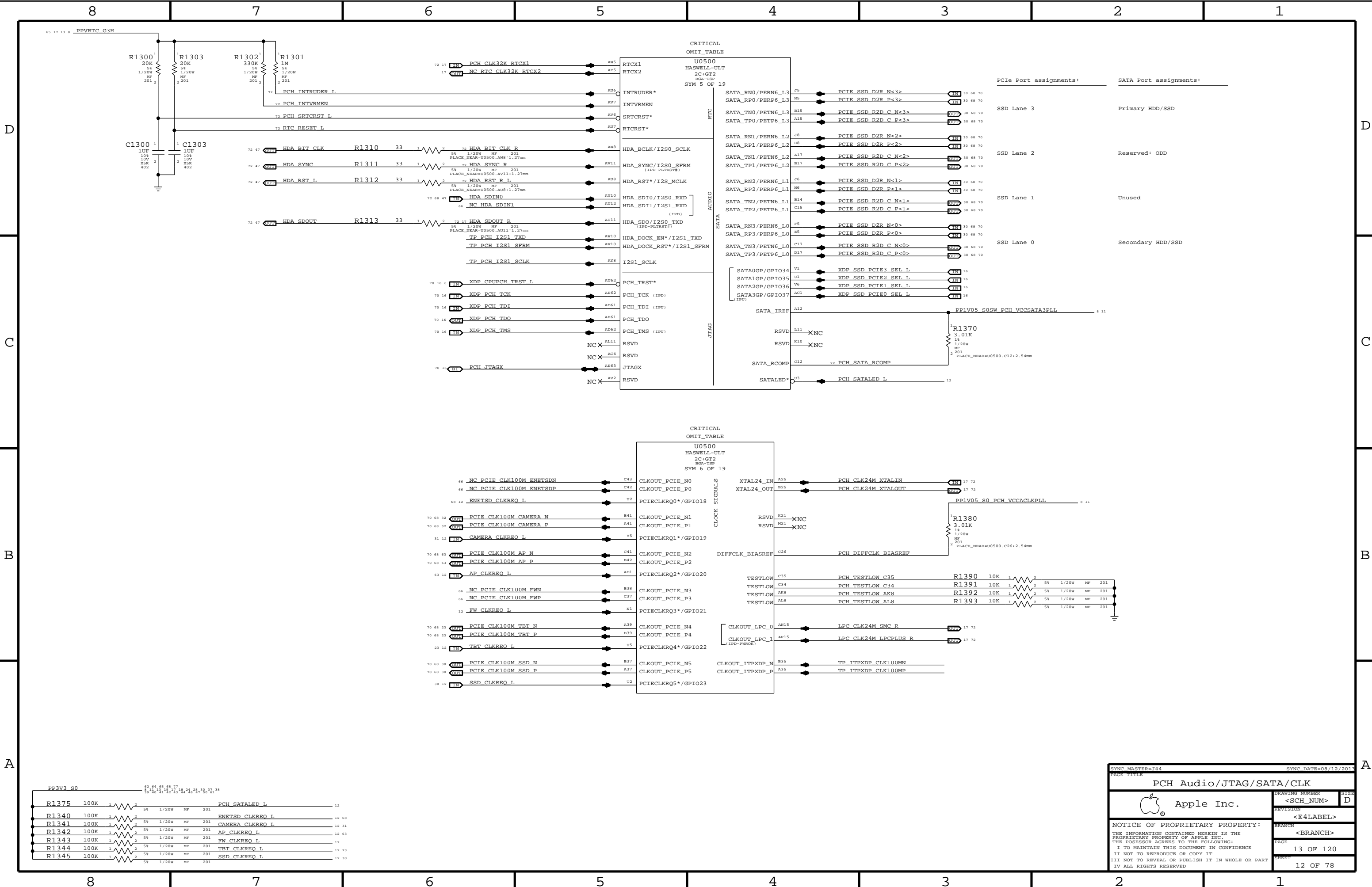




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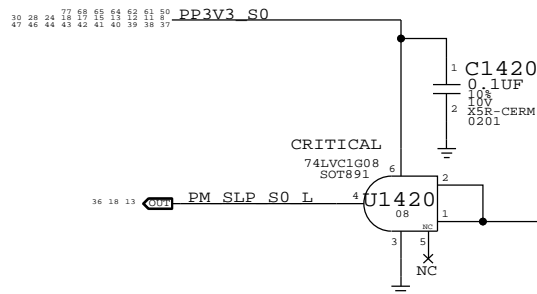
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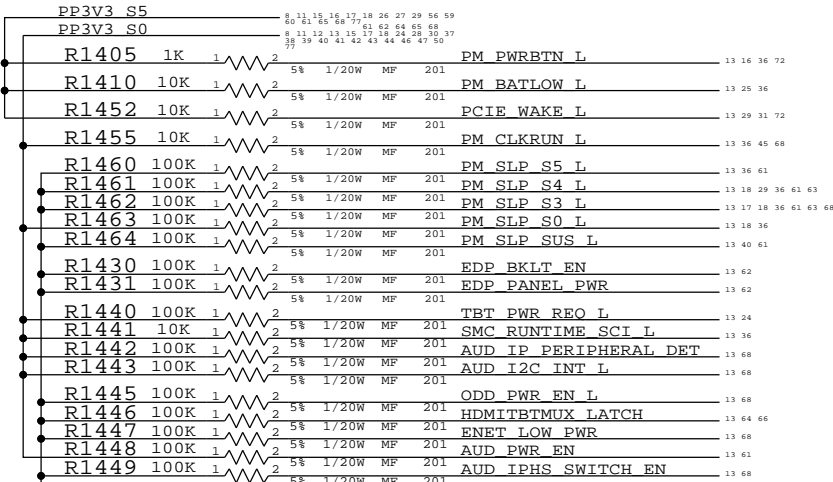
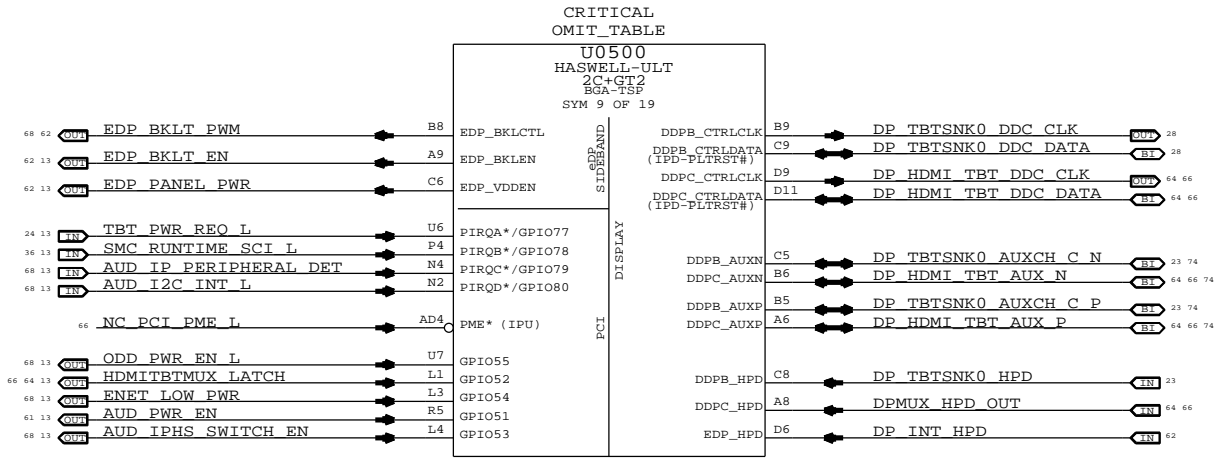
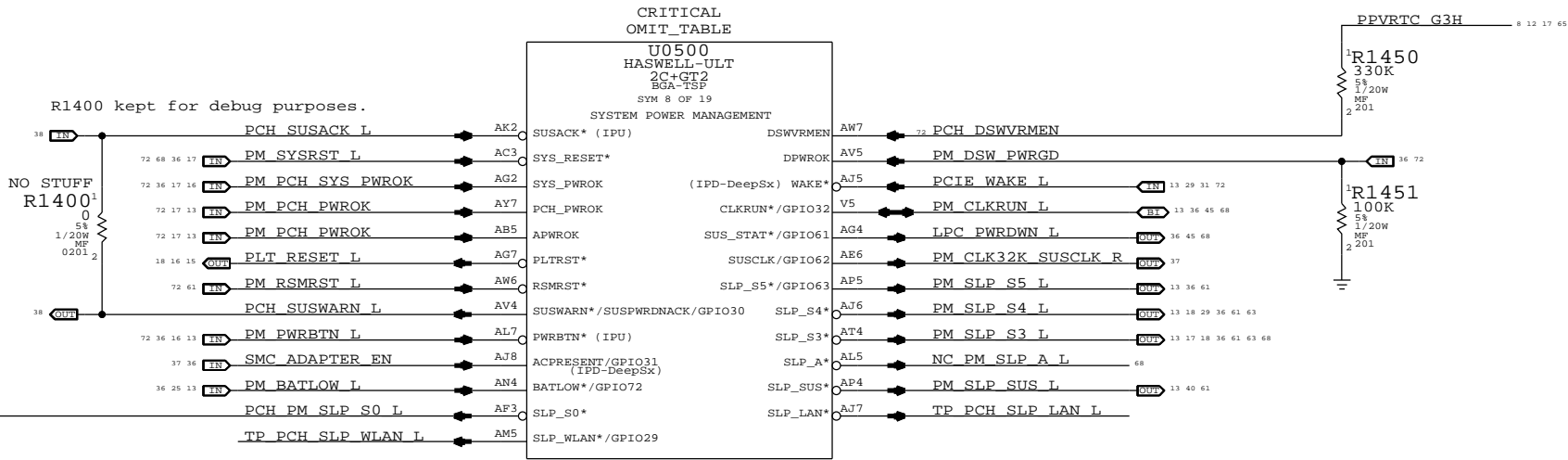
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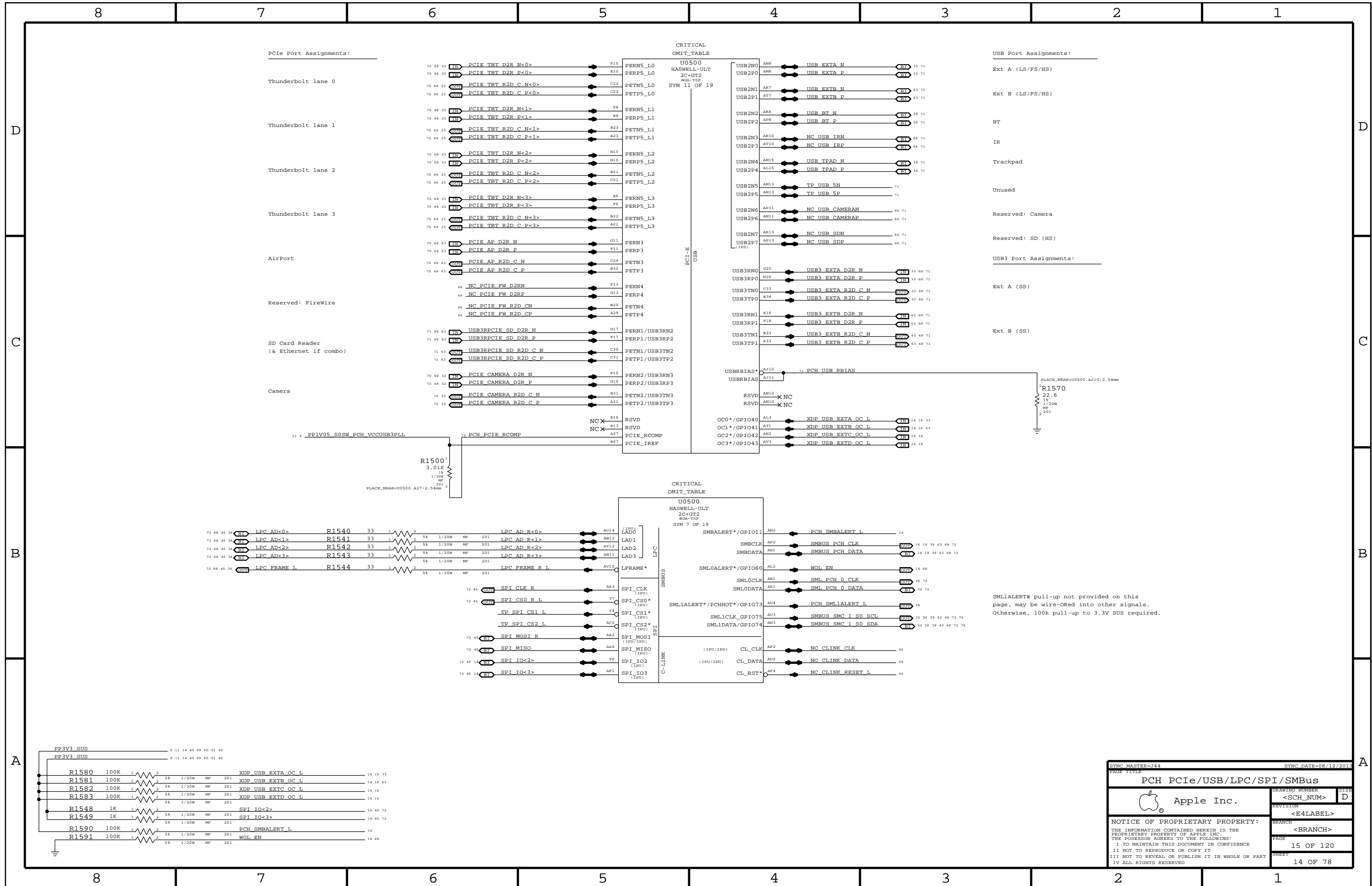
SLP_S0# Isolation

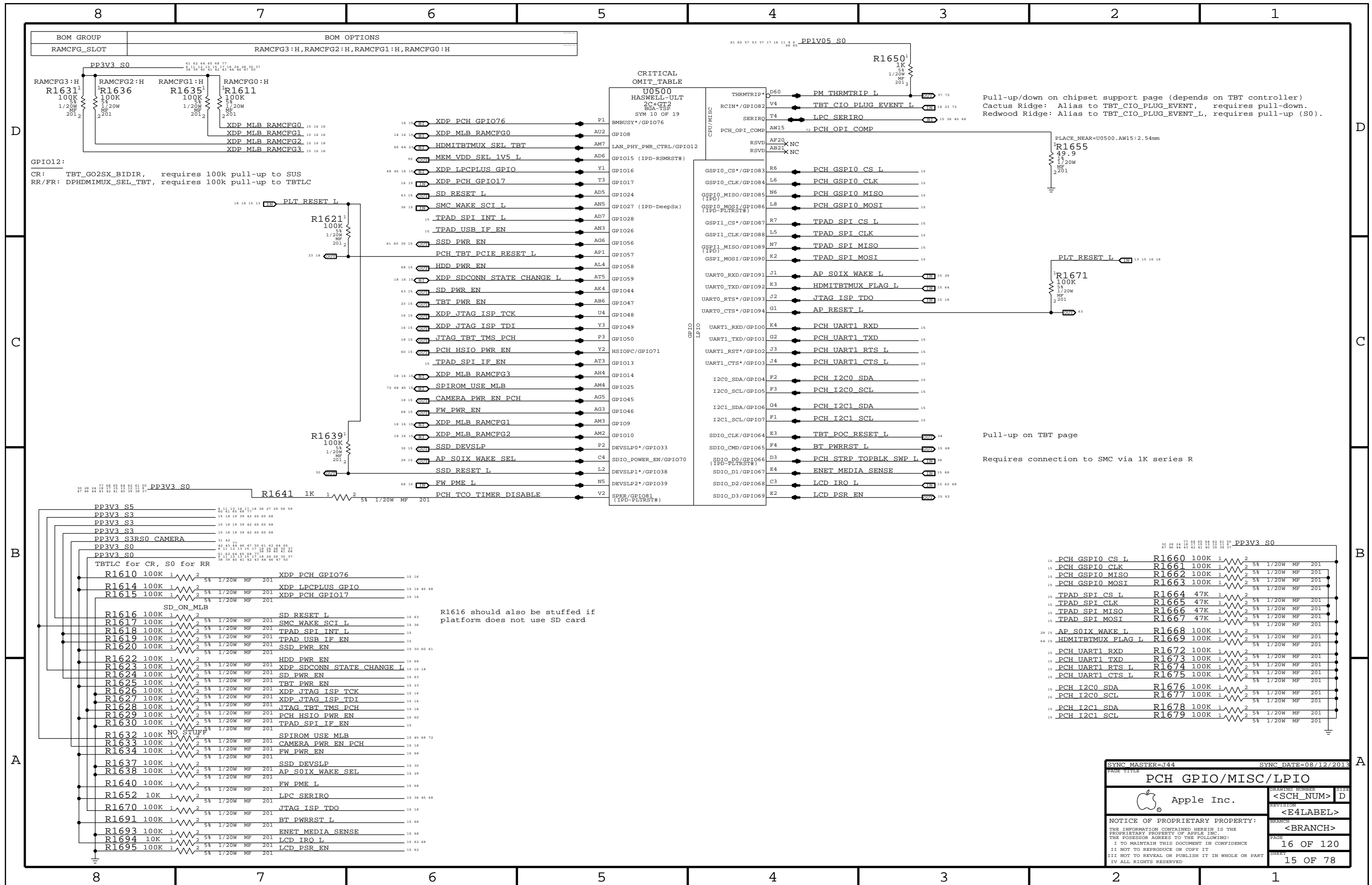


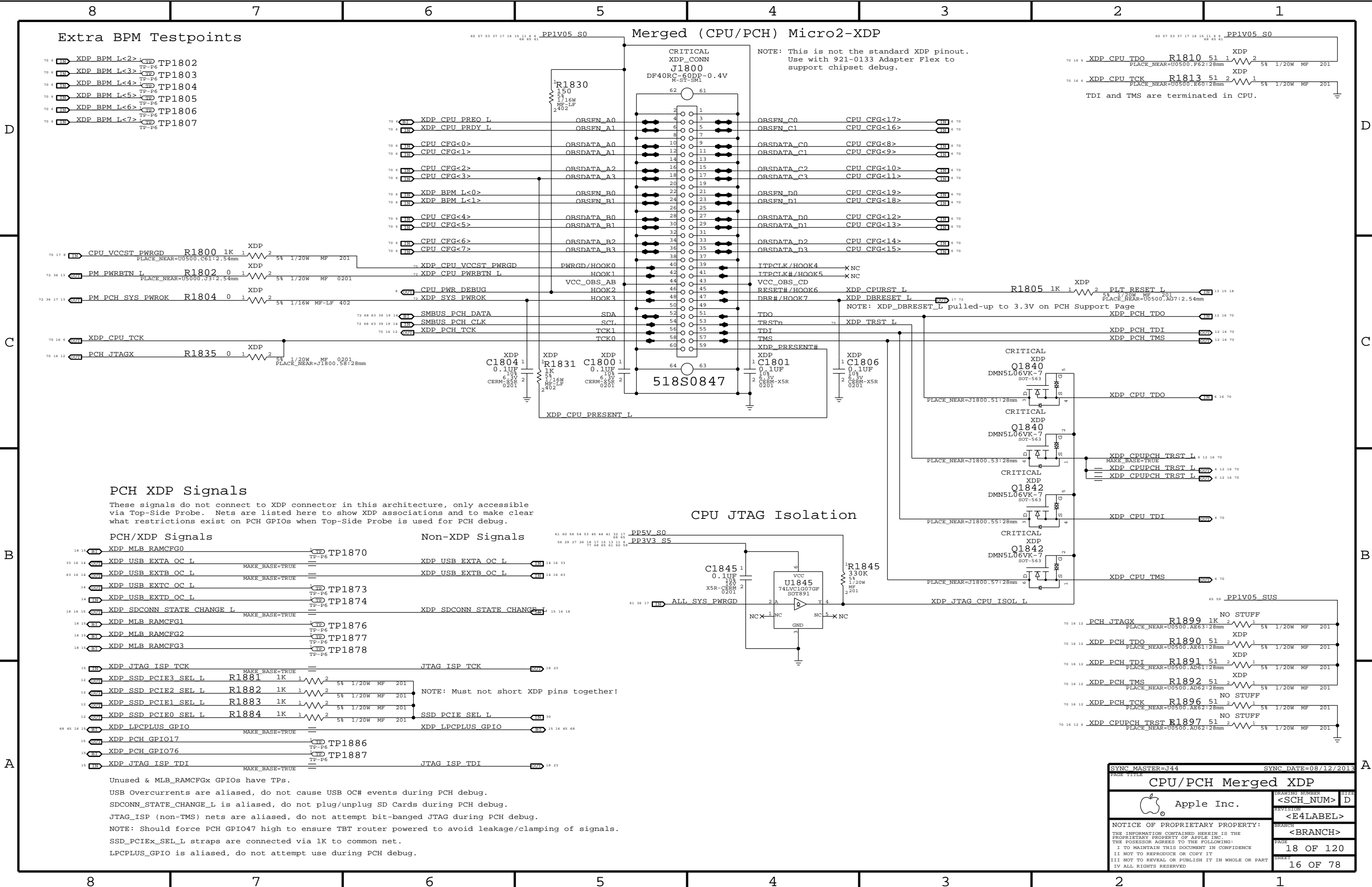
SLP_S0# can be driven high outside of S0
U1420 ensures signal will only be high in S0.



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PCH PM/PCI/GFX			
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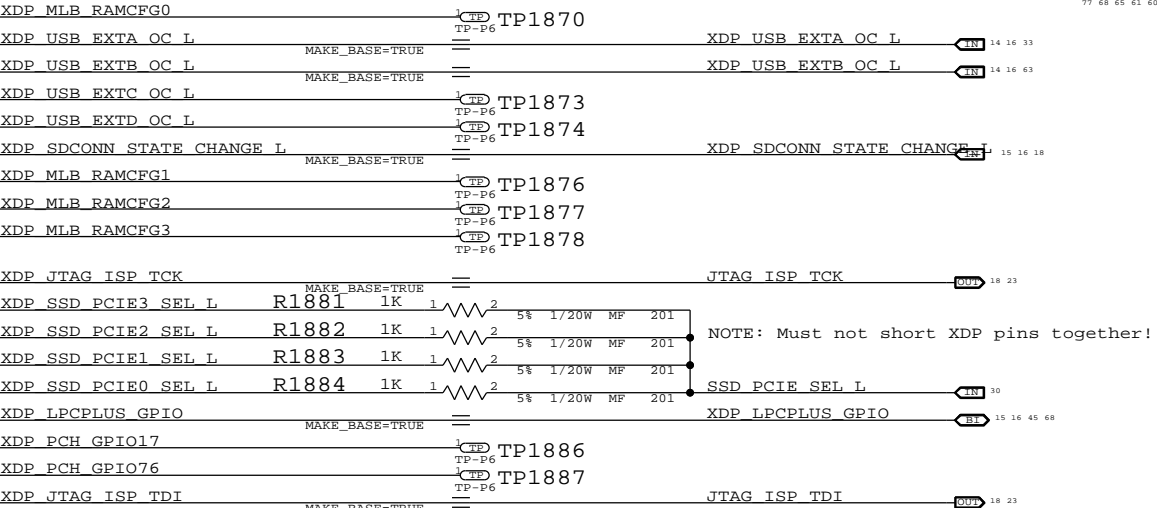


PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals

Non-XDP Signals



Unused & MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.


SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

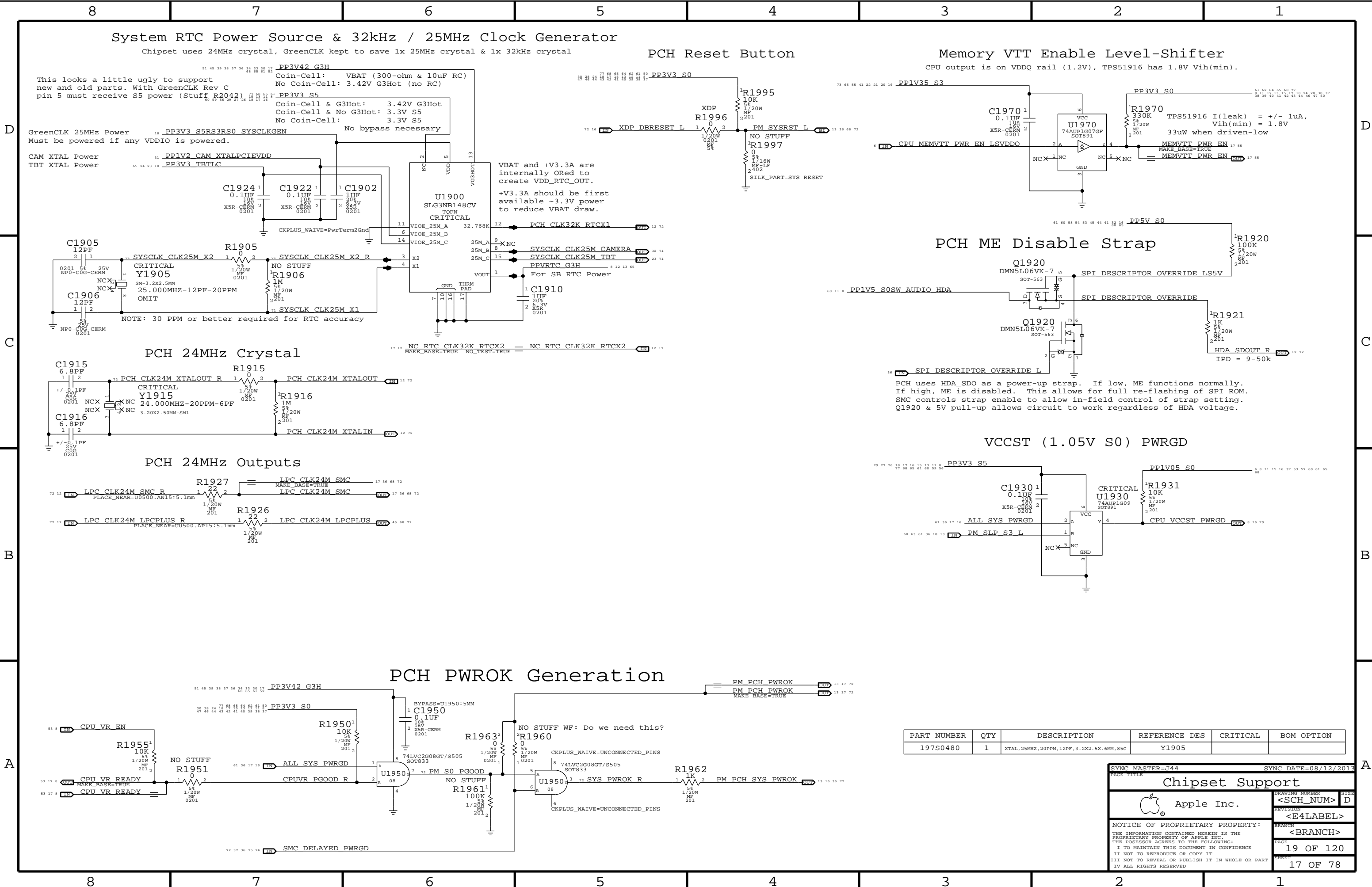
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

SSD_PCIEx_SEL_L straps are connected via 1K to common net.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

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CPU/PCH Merged XDP			
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System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

This looks a little ugly to support new and old parts. With GreenCLK Rev C pin 5 must receive S5 power (Stuff R2042)

GreenCLK 25MHz Power Must be powered if any VDDIO is powered.

CAM XTAL Power
TBT XTAL Power

PP3V42 G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)
PP3V3 S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

VBAT and +V3.3A are internally ORED to create VDD_RTC_OUT.
+V3.3A should be first available ~3.3V power to reduce VBAT draw.

NOTE: 30 PPM or better required for RTC accuracy

PCH 24MHz Crystal

PCH 24MHz Outputs

PCH Reset Button

Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).


PCH ME Disable Strap

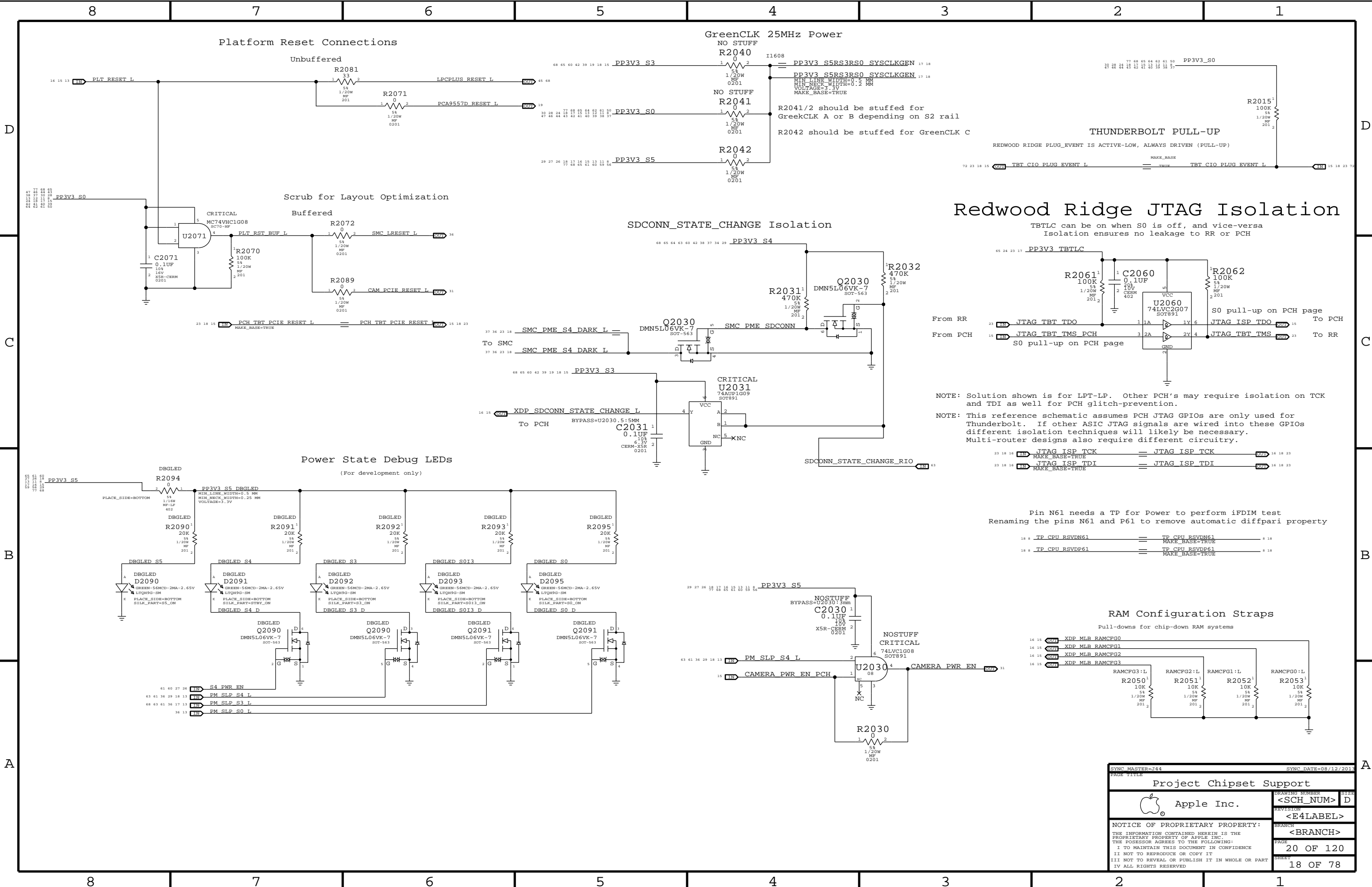
PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD

PCH PWROK Generation

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0480	1	XTAL, 25MHZ, 20PPM, 12PF, 3.2X2.5X.6MM, 85C	Y1905		

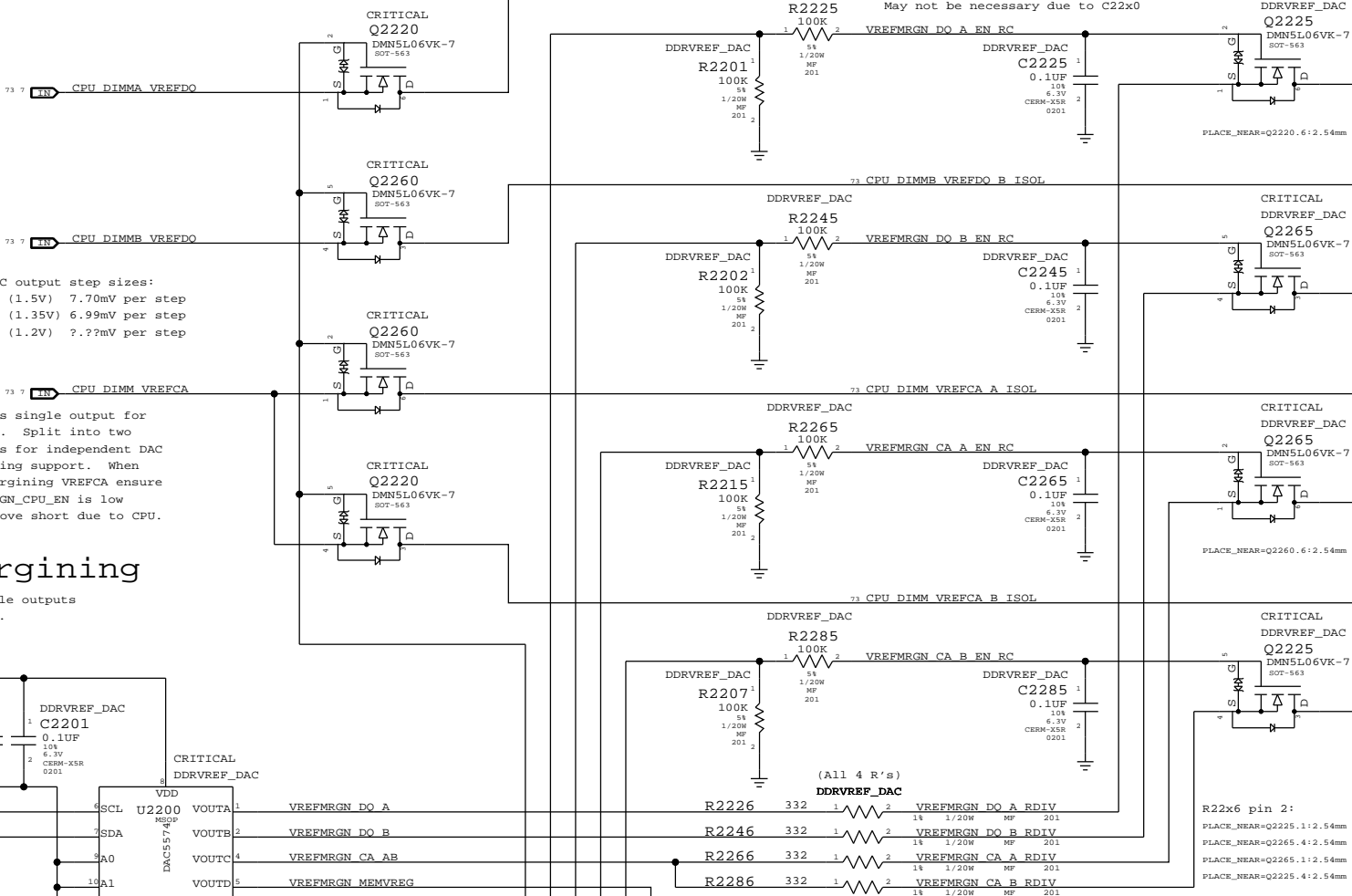
SYNC MASTER=J44		SYNC DATE=08/12/2013	
PAGE TITLE			
Chipset Support			
		Apple Inc.	
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		<SCH_NUM>	
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<BRANCH>			
PAGE		19 OF 120	
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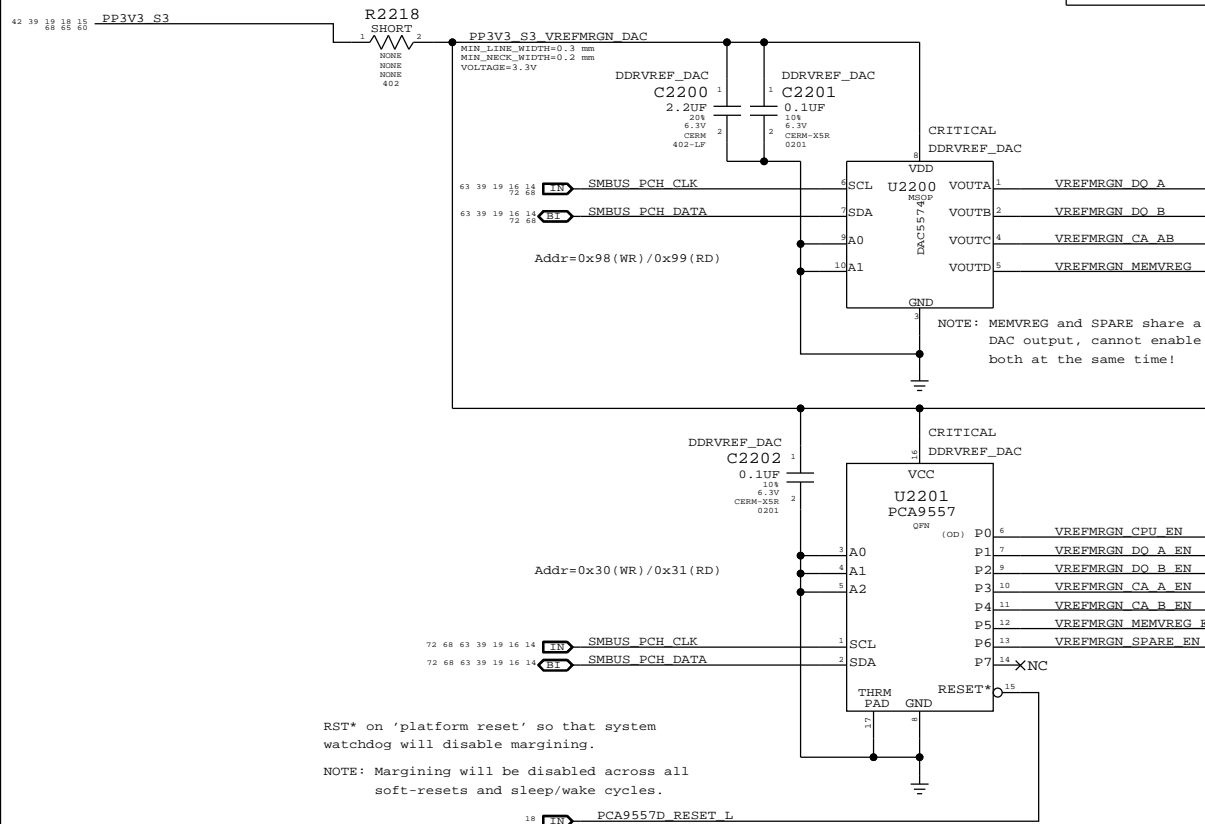
BOM options provided by this page:

- DDRVREF DAC - Stuffs DAC margining circuit.

FETs for CPU isolation during DAC margining



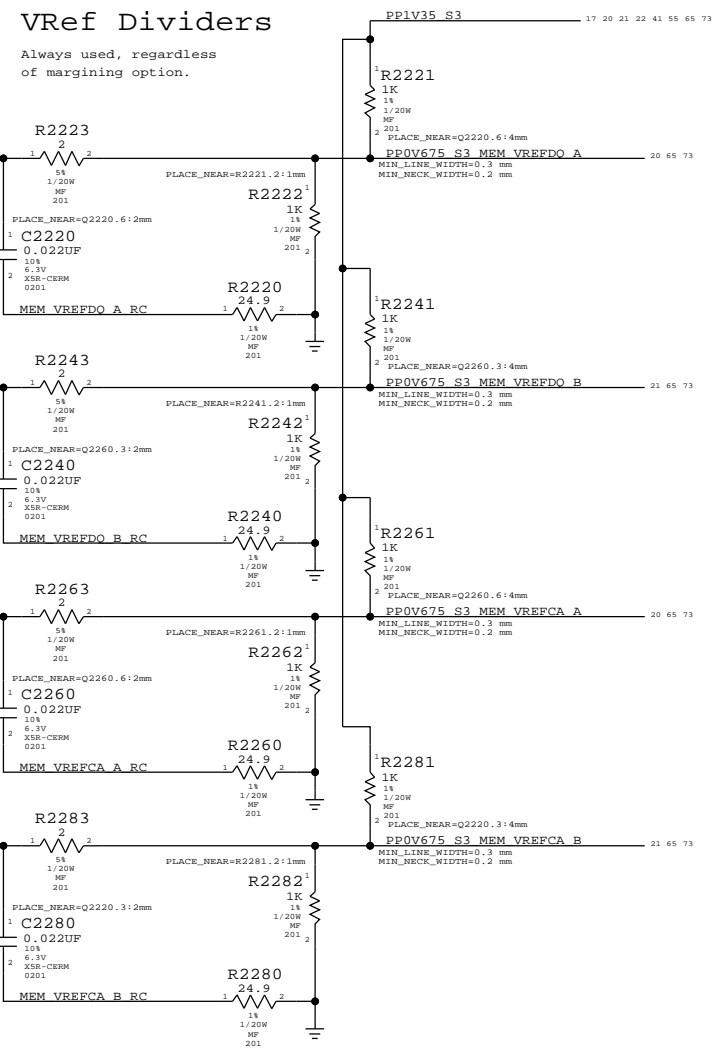
DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.




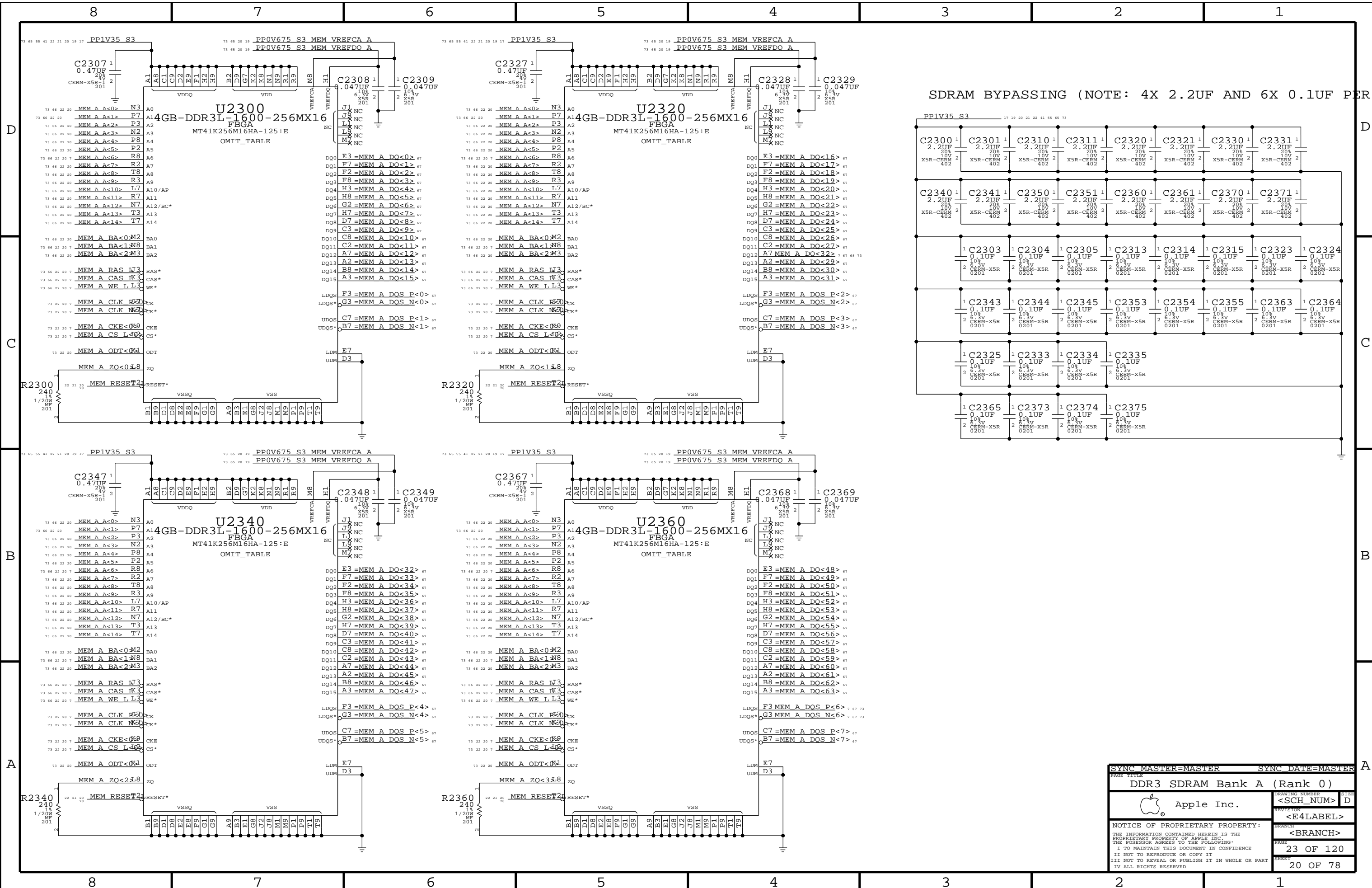
	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V) DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D) 1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV) 0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA) 0.000V - 2.694V (0x00 - 0xD1)
Vref current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced) +25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output 3.53mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider


Always used, regardless
of margining option.



SYNC MASTER=J44		SYNC DATE=08/12/2011	
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DDR3 VREF MARGINING			
 Apple Inc.		DRAWING NUMBER	SIZ
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SDRAM BYPASSING (NOTE: 4X 2.2UF AND 6X 0.1UF PER CHIP)

SYNC MASTER=MASTER		SYNC DATE=MASTER			
PAGE TITLE					
DDR3 SDRAM Bank A (Rank 0)					
	DRAWING NUMBER		SIZE		
	<SCH_NUM>		D		
	REVISION		<E4LABEL>		
	BRANCH		<BRANCH>		
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MEM_ODT:CPU drives ODT from CPU, terminated to 0.675V VTT.
MEM_ODT:PU disconnect ODT from CPU, ODT pins on DRAM pulled up to 1.35V VDDQ.



Reset is an open drain in Haswell ULT and needs pull up



Place Source C termination before first DRAM



```
Place RC end termination after last DRAM
```

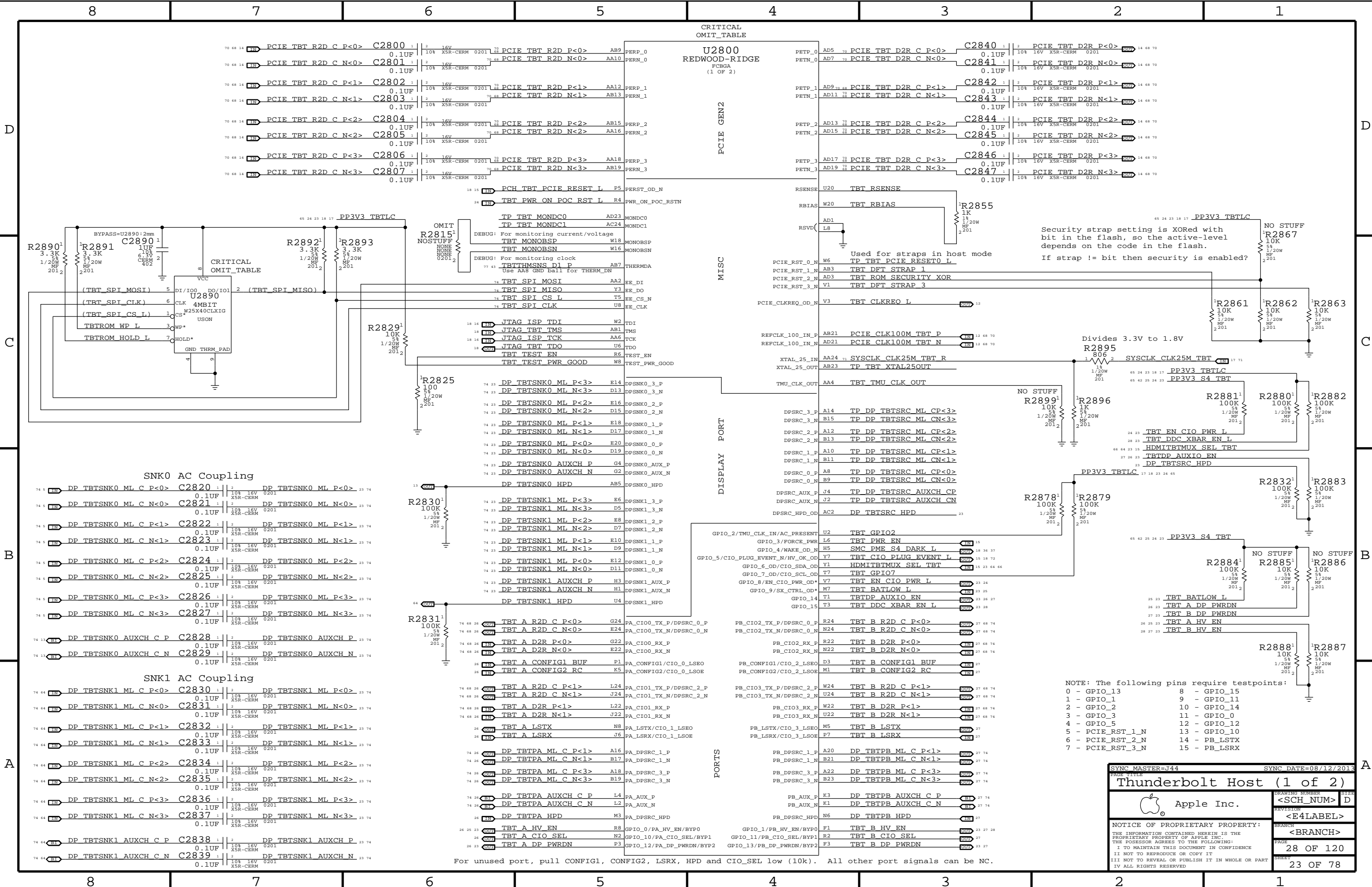


73 68 65 55 22 PP0V675 S0 DDRVTI

73 68 65 55 22 PP0V675 S0 DDRVTI

D

A



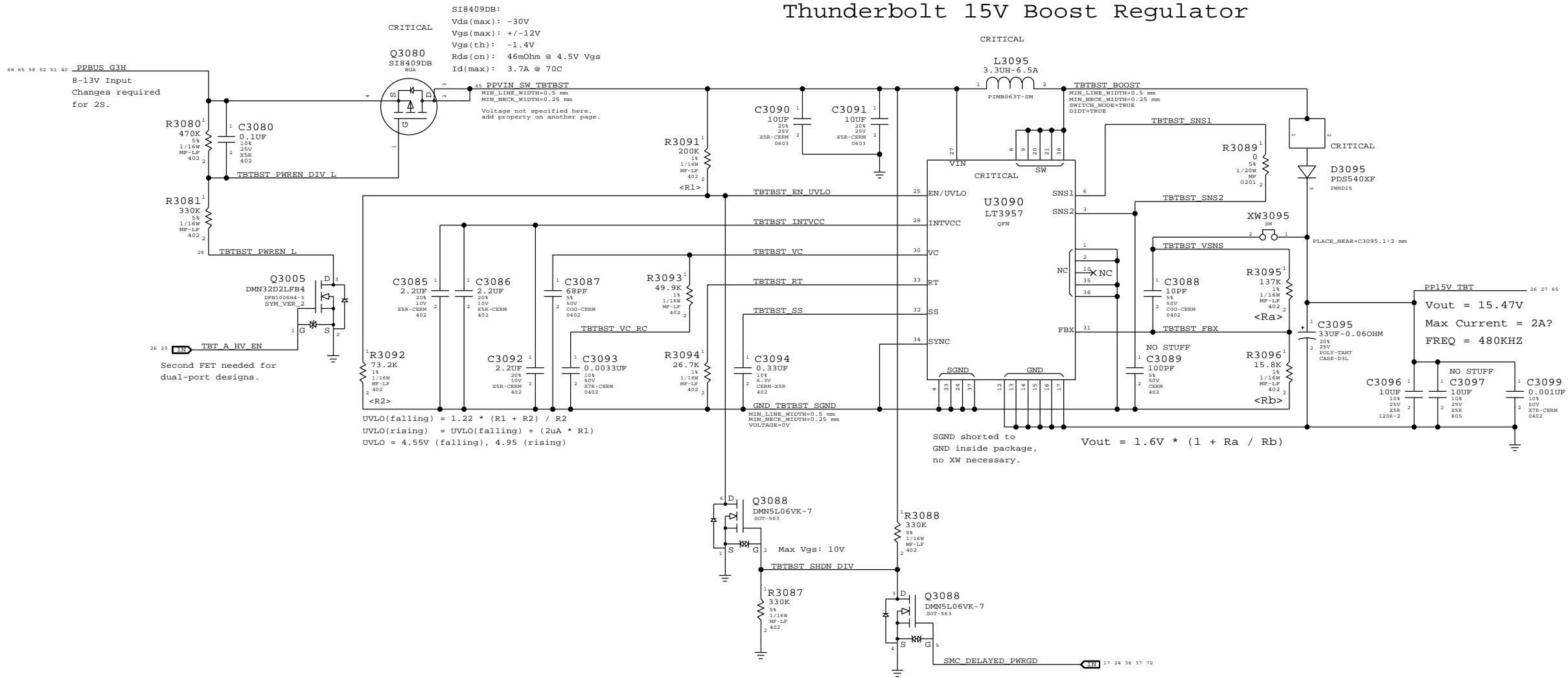
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

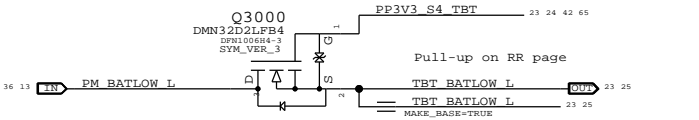
Signal aliases required by this page:
(NONE)


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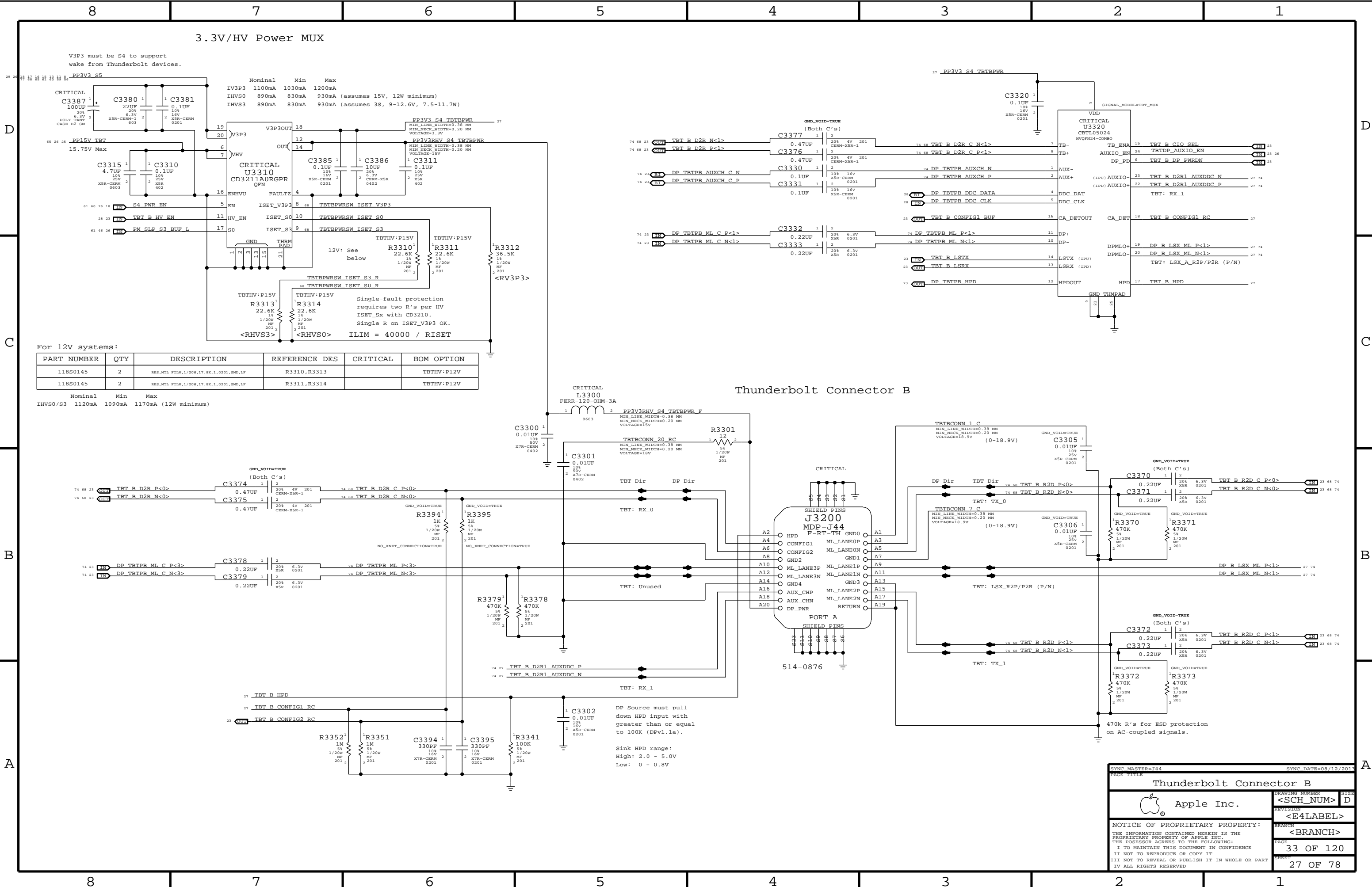
Thunderbolt 15V Boost Regulator



BATLOW# Isolation



SYNC MASTER=J44		SYNC DATE=08/12/2013	
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Thunderbolt Mobile Support		DRAWING NUMBER	
 Apple Inc.		<SCH_NUM>	
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Thunderbolt Connector B

D

C

B

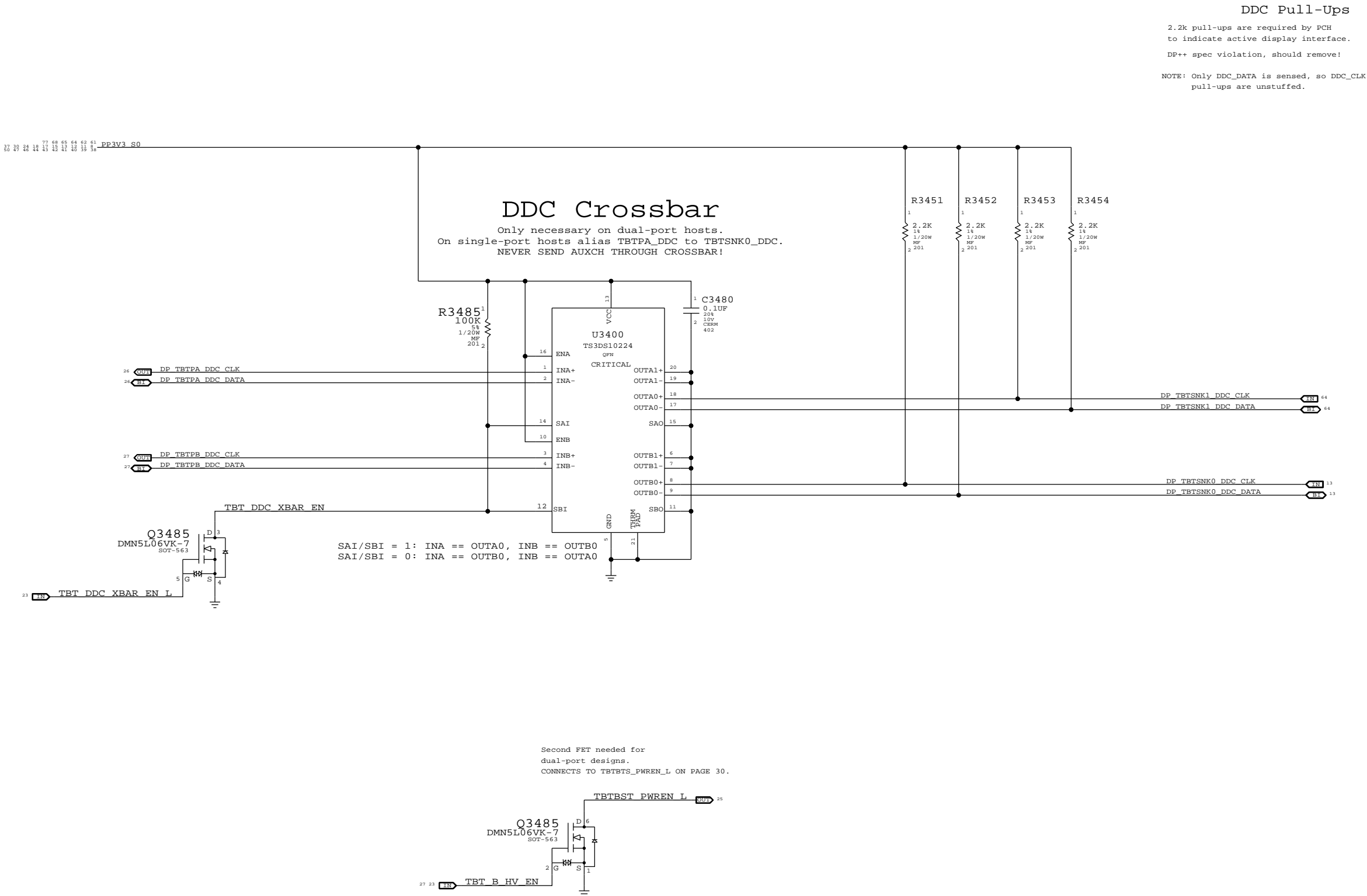
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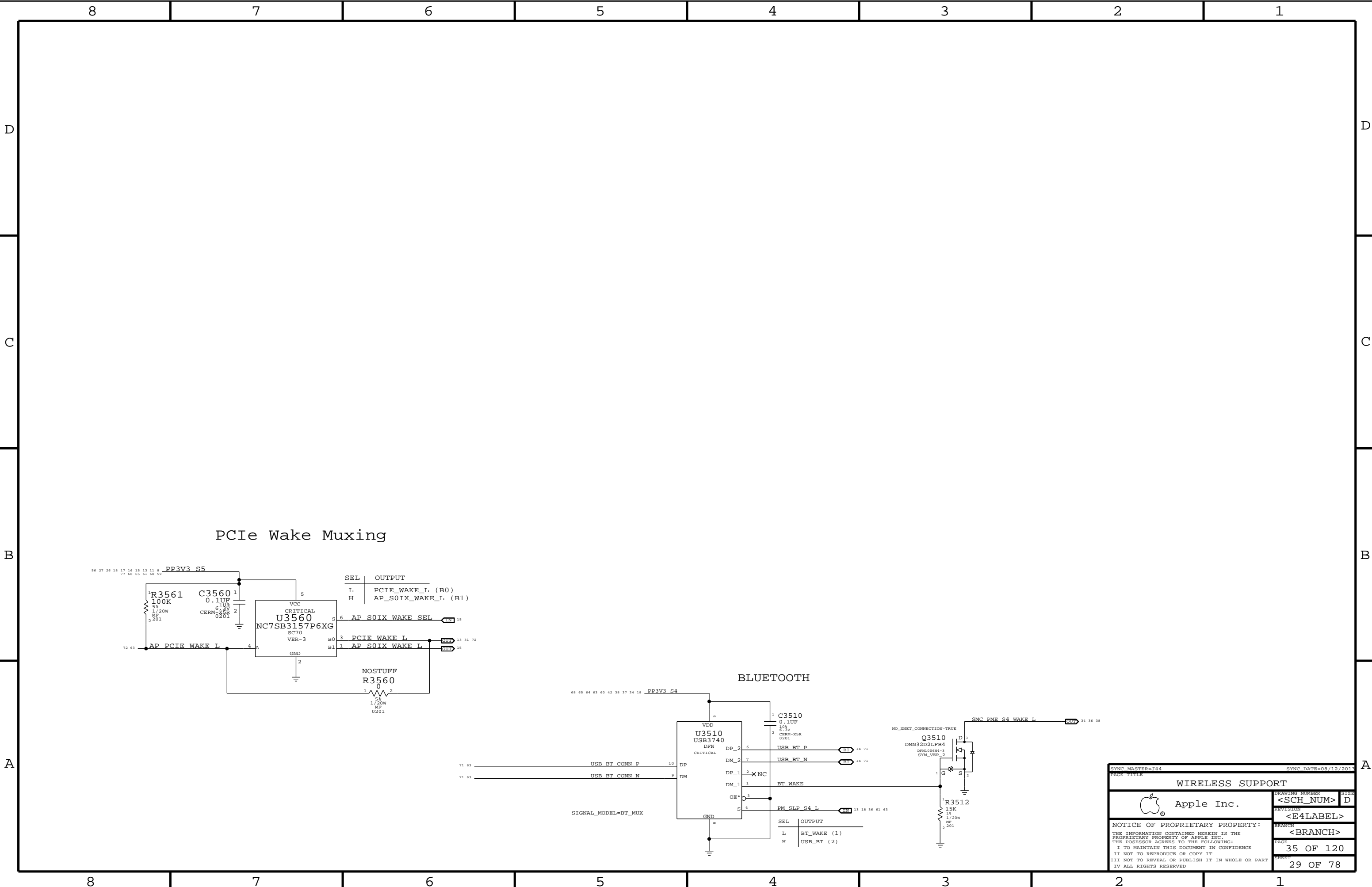
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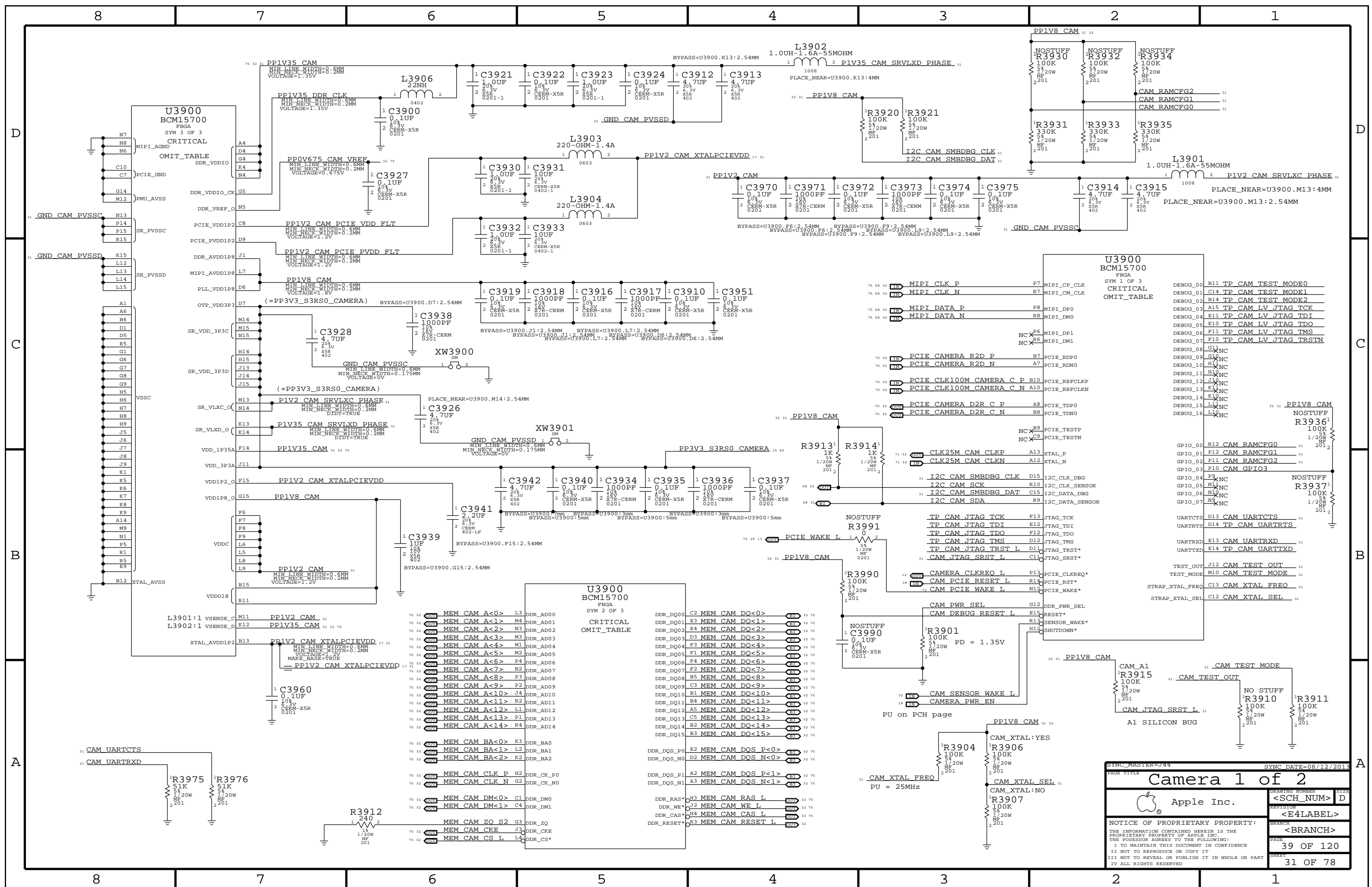
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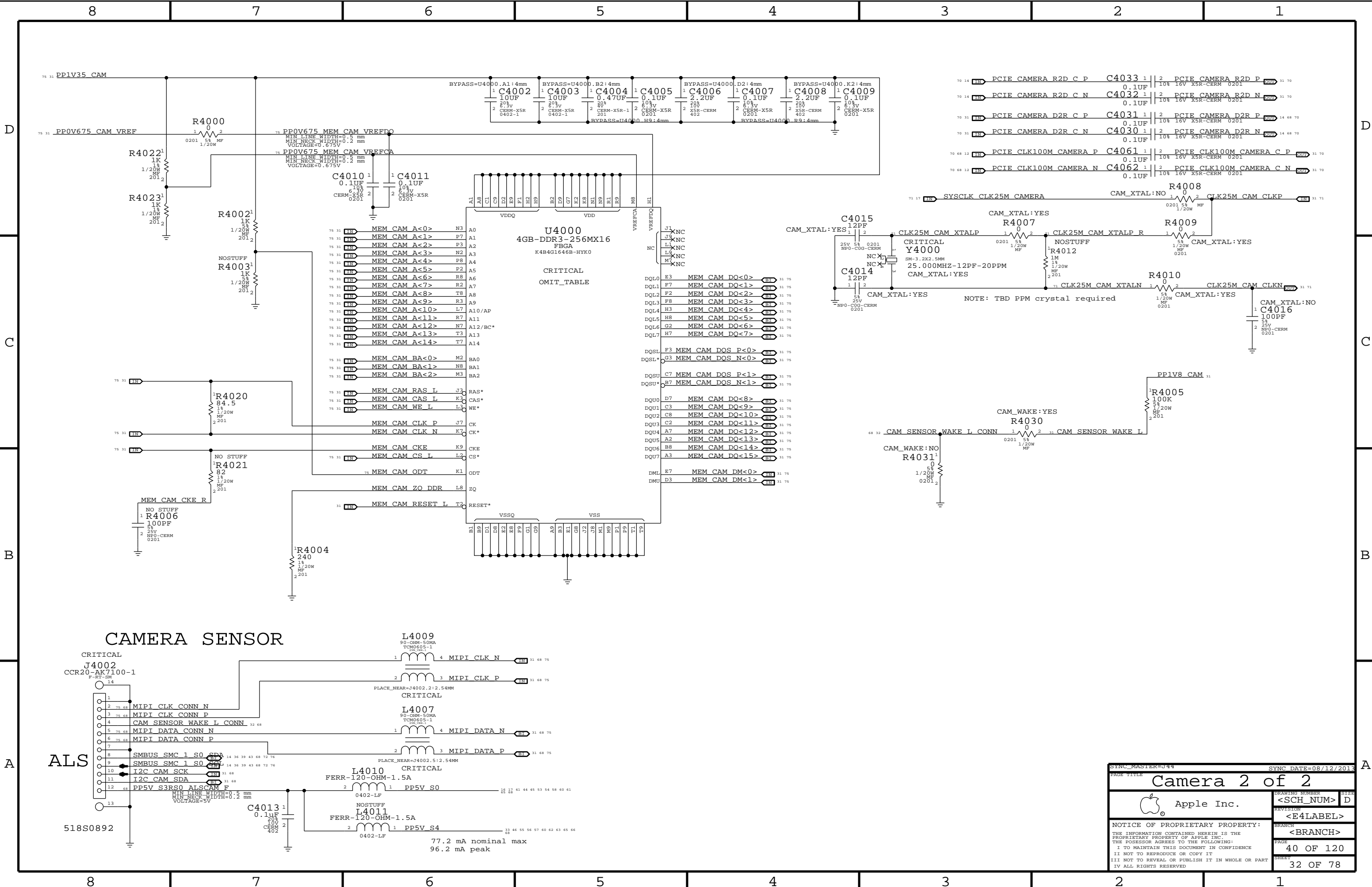
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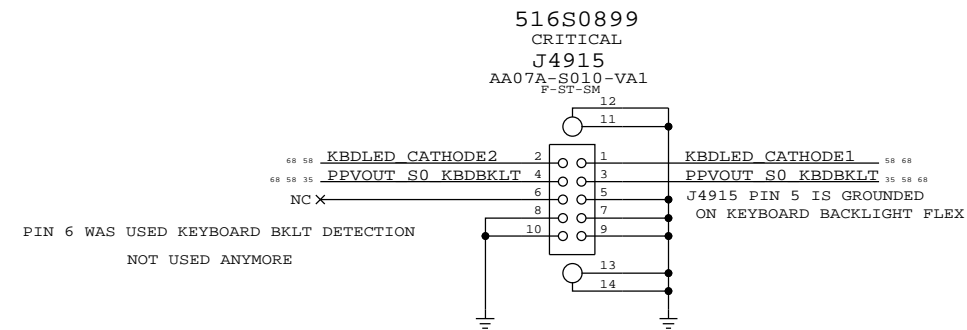
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DDC Crossbar			
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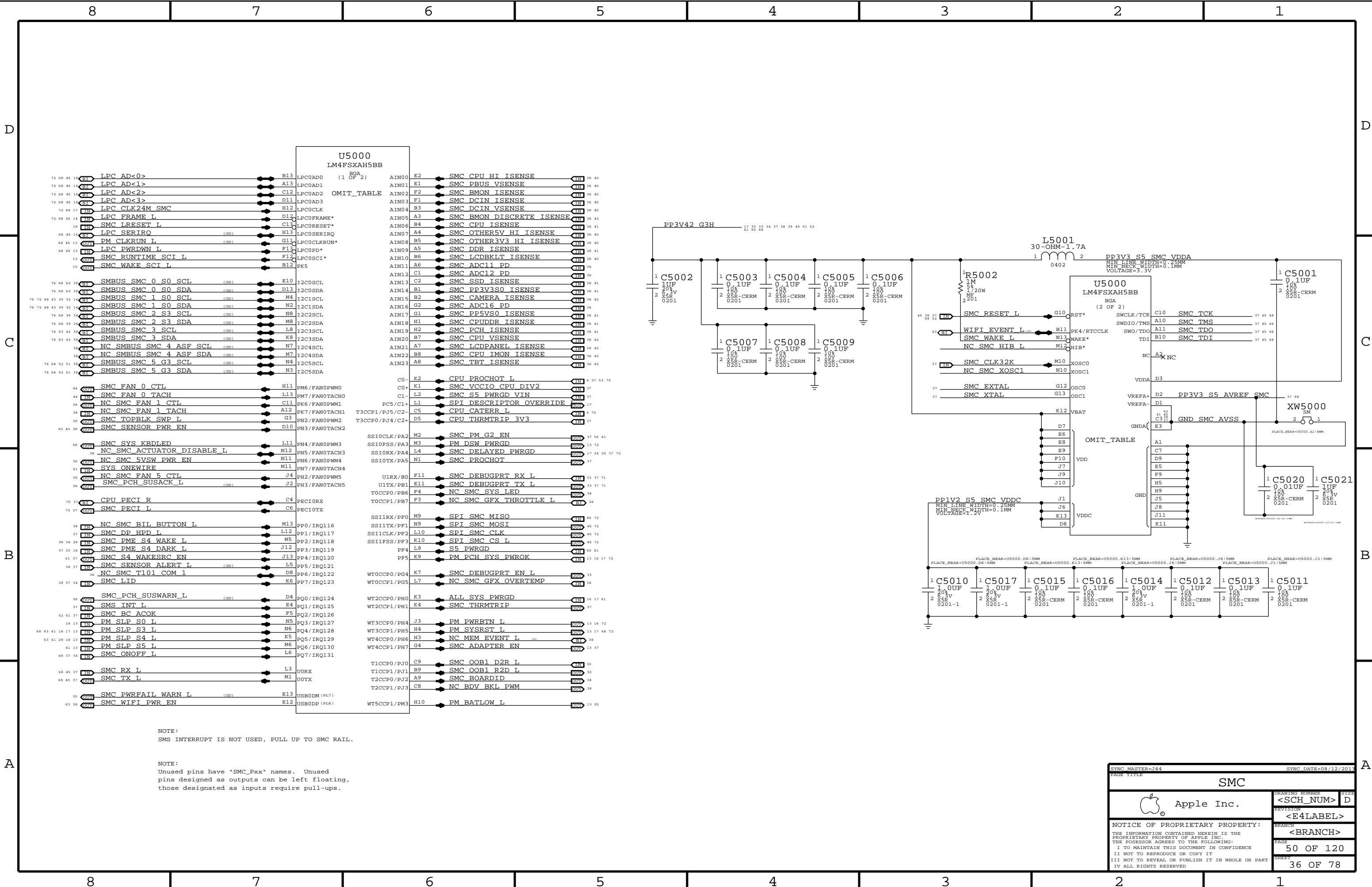


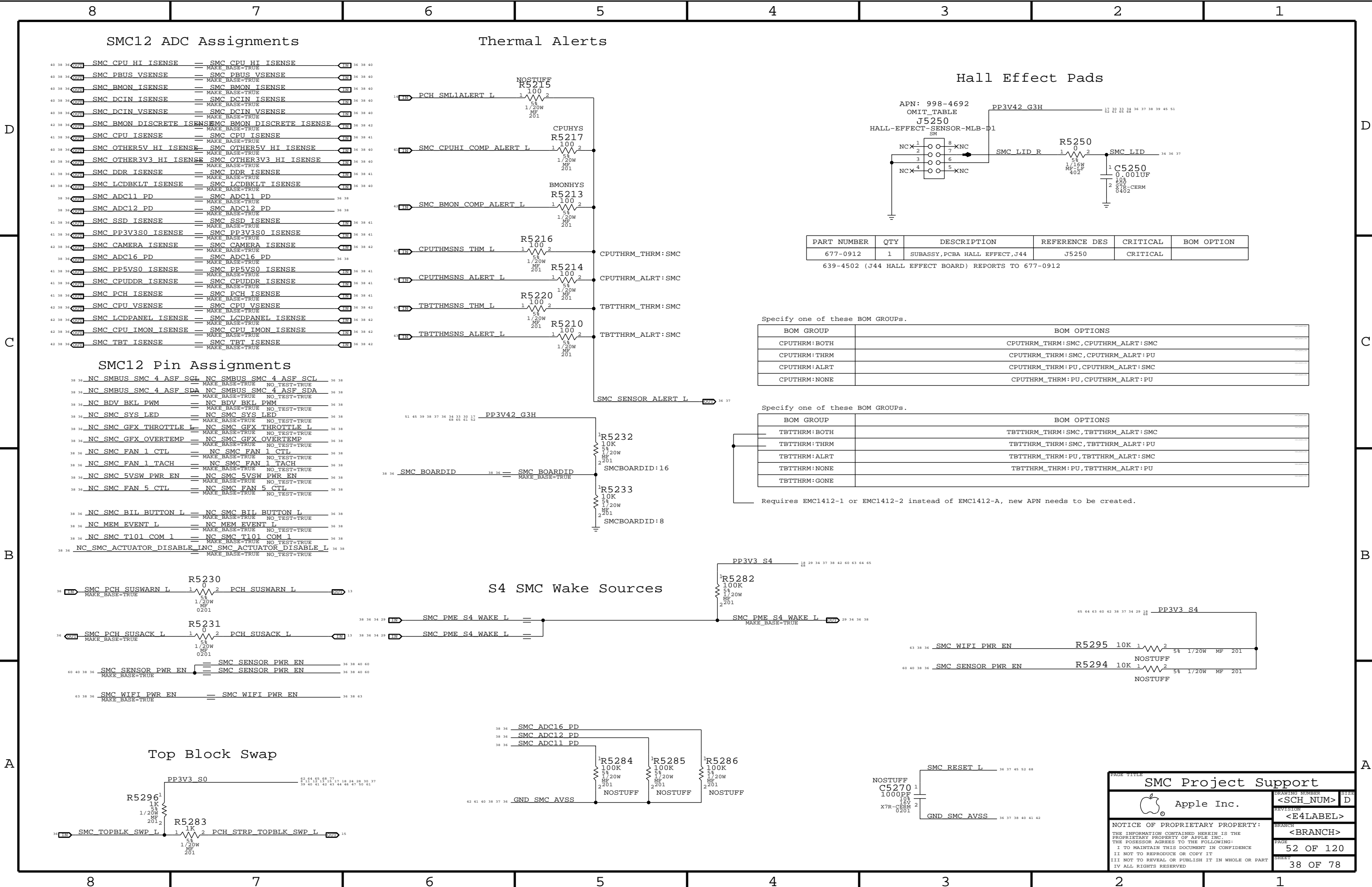


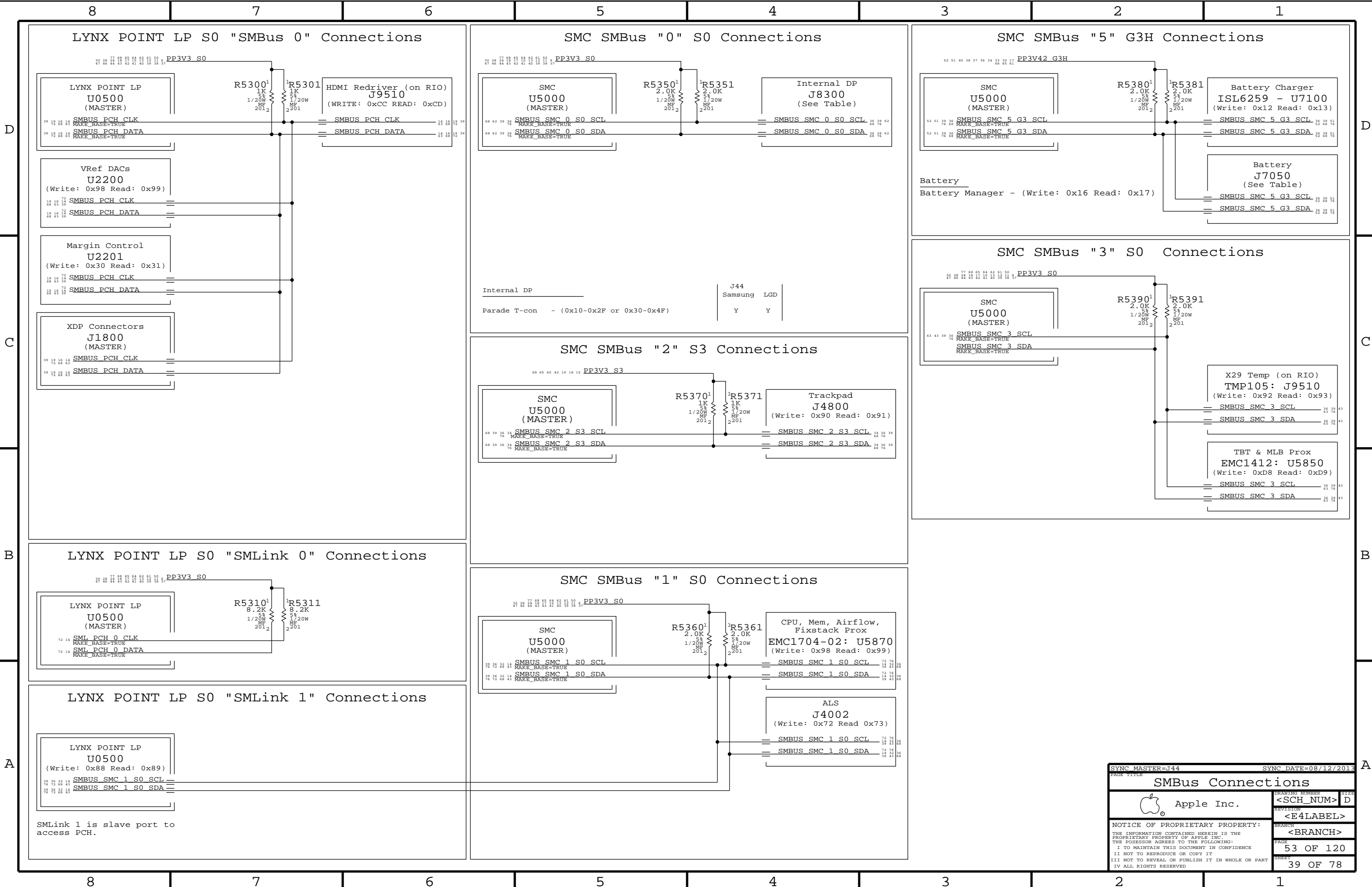



Keyboard Backlight Connector

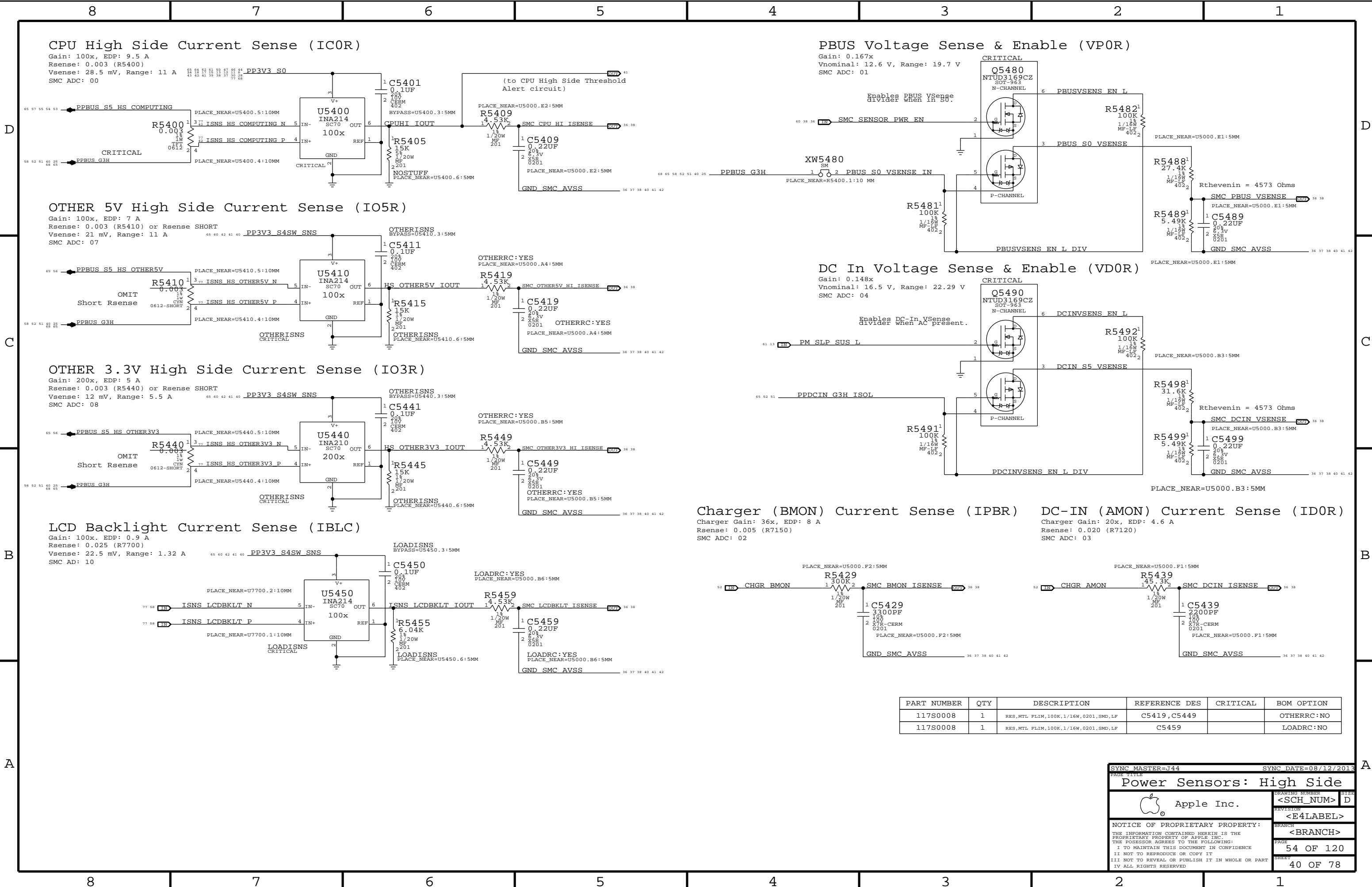








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SMBus Connections			
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		PAGE	53 OF 120
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CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 9.5 A
Rsense: 0.003 (R5400)
Vsense: 28.5 mV, Range: 11 A
SMC ADC: 00

OTHER 5V High Side Current Sense (IO5R)

Gain: 100x, EDP: 7 A
Rsense: 0.003 (R5410) or Rsense SHORT
Vsense: 21 mV, Range: 11 A
SMC ADC: 07

OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 5 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 12 mV, Range: 5.5 A
SMC ADC: 08

LCD Backlight Current Sense (IBLC)

Gain: 100x. EDP: 0.9 A
Rsense: 0.025 (R7700)
Vsense: 22.5 mV, Range: 1.32 A
SMC AD: 10

PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 19.7 V
SMC ADC: 01

DC In Voltage Sense & Enable (VD0R)

Gain: 0.148x
Vnominal: 16.5 V, Range: 22.29 V
SMC ADC: 04


Charger (BMON) Current Sense (IPBR)

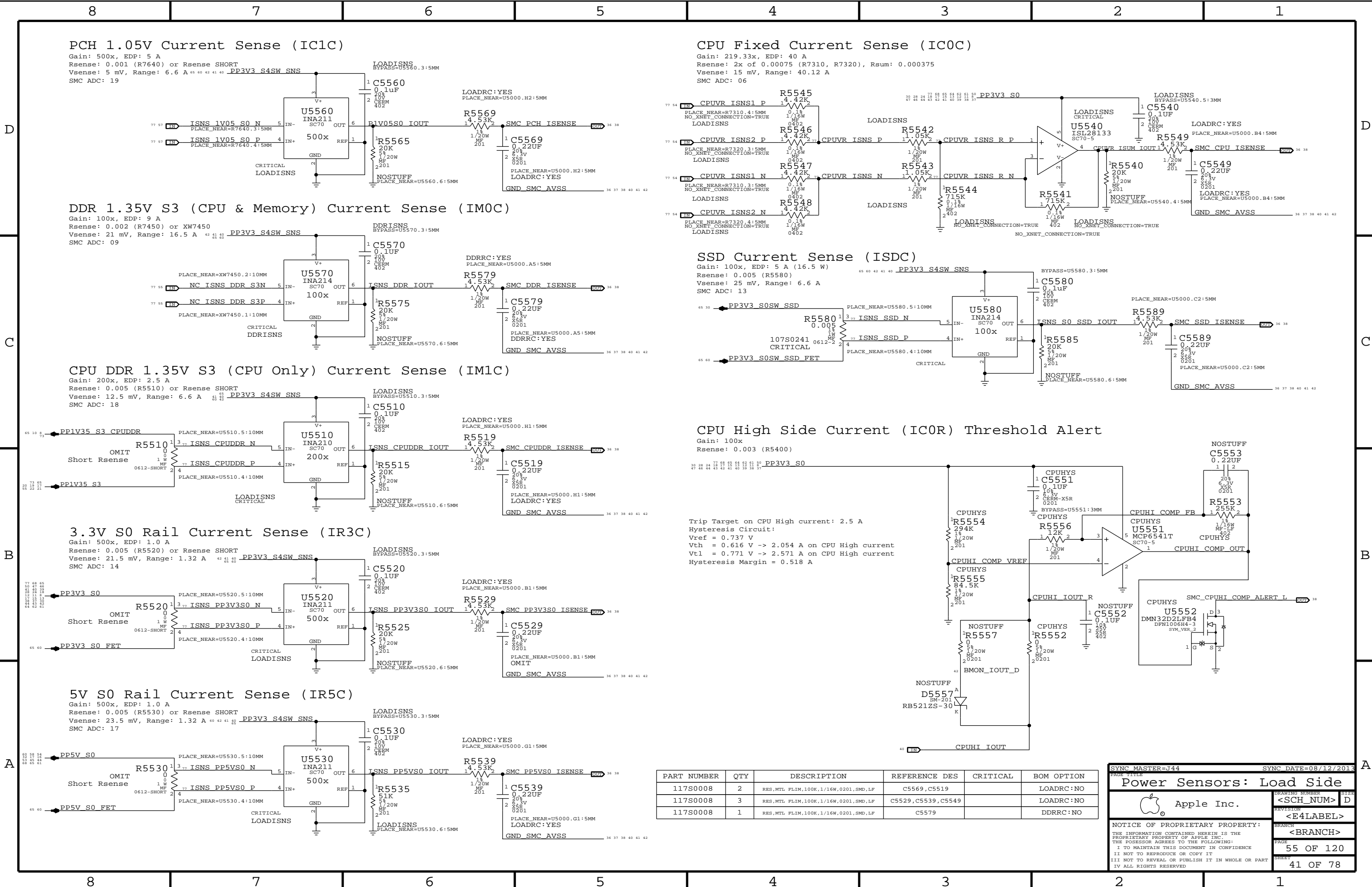
Charger Gain: 36x, EDP: 8 A
Rsense: 0.005 (R7150)
SMC ADC: 02

DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7120)
SMC ADC: 03

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		OTHERRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO

SYNC MASTER=J44		SYNC DATE=08/12/2013	
PAGE TITLE			
Power Sensors: High Side			
 Apple Inc.		DRAWING NUMBER	SIZE
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519		LOADRC:NO
117S0008	3	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5529,C5539,C5549		LOADRC:NO
117S0008	1	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

SYNC MASTER=J44

SYNC DATE=08/12/2013

PAGE TITLE

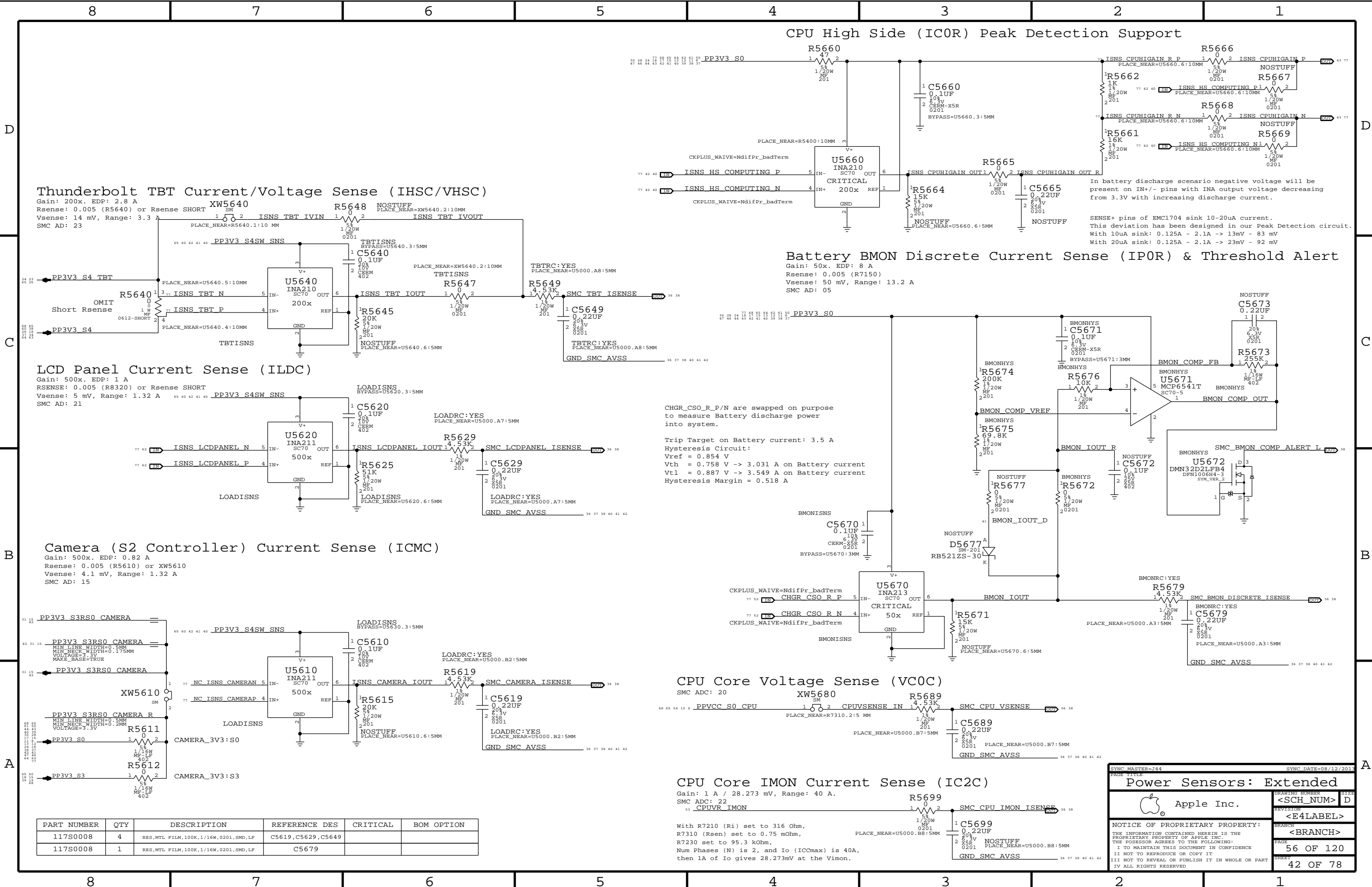
Power Sensors: Load Side

 Apple Inc.

DRAWING NUMBER
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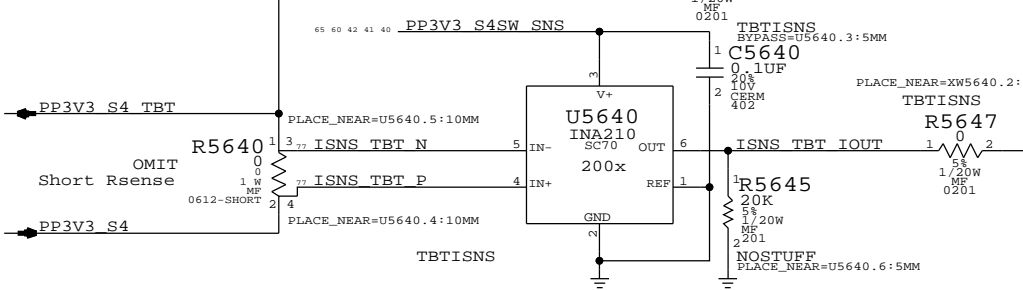
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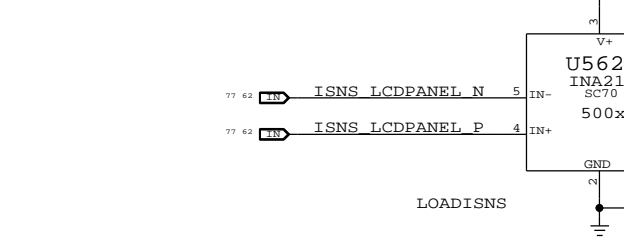
Thunderbolt TBT Current/Voltage Sense (IHSC/VHSC)

Gain: 200x. EDP: 2.8 A
Rsense: 0.005 (R5640) or Rsense SHORT
Vsense: 14 mV, Range: 3.3 A
SMC AD: 23



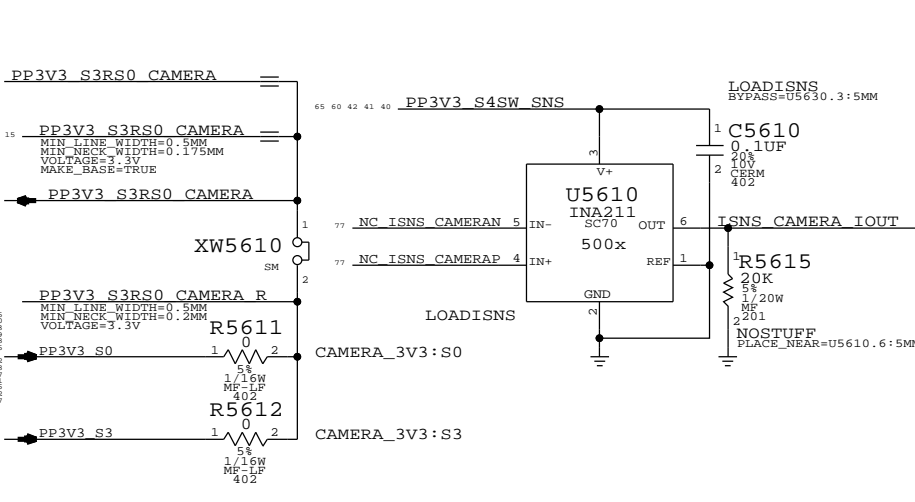
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
RSENSE: 0.005 (R8320) or Rsense SHORT
Vsense: 5 mV, Range: 1.32 A
SMC AD: 21



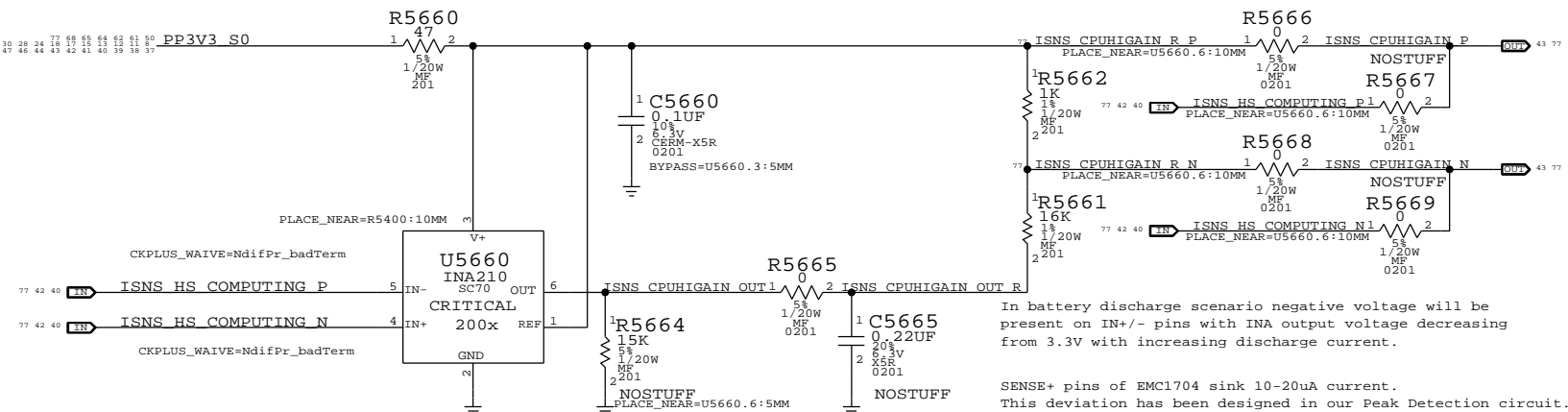
Camera (S2 Controller) Current Sense (ICMC)

Gain: 500x. EDP: 0.82 A
Rsense: 0.005 (R5610) or XW5610
Vsense: 4.1 mV, Range: 1.32 A
SMC AD: 15



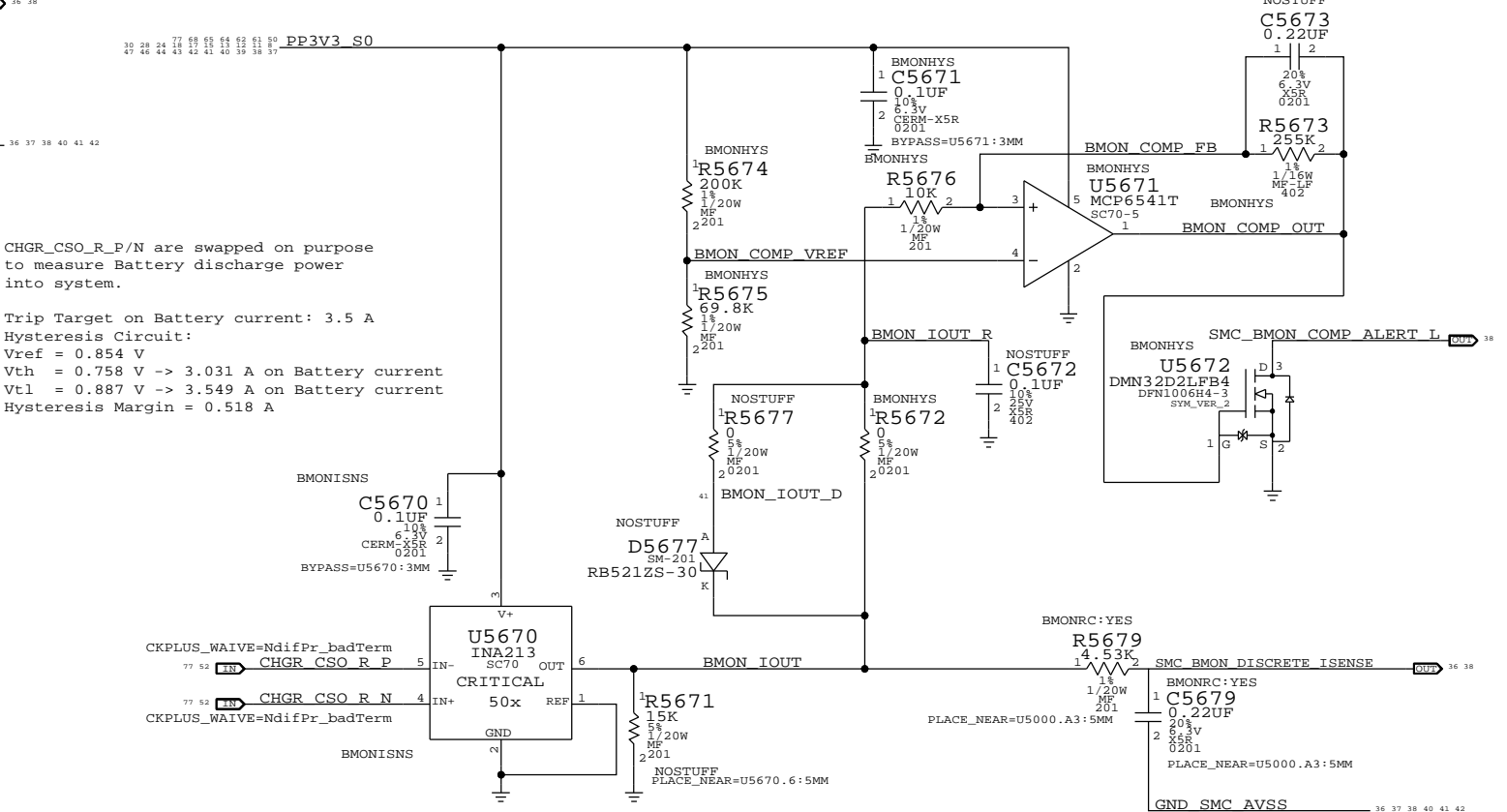
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629,C5649		
117S0008	1	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5679		

CPU High Side (IC0R) Peak Detection Support



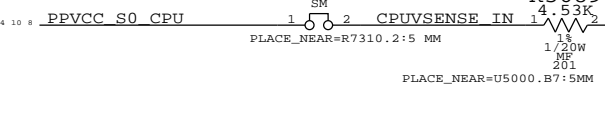
Battery BMON Discrete Current Sense (IP0R) & Threshold Alert

Gain: 50x. EDP: 8 A
Rsense: 0.005 (R7150)
Vsense: 50 mV, Range: 13.2 A
SMC AD: 05



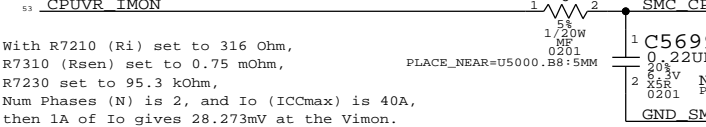
CPU Core Voltage Sense (VC0C)

SMC ADC: 20



CPU Core IMON Current Sense (IC2C)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 22



SYNC MASTER=J44

SYNC DATE=08/12/2013

Power Sensors: Extended

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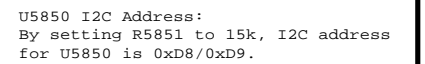
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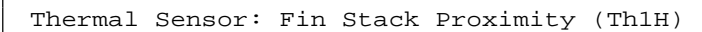
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I2C Write: 0xD8, I2C Read: 0xD9



Thermal Diode: MLB Proximity (TMLB)

I2C Write: 0x98, I2C Read: 0x99

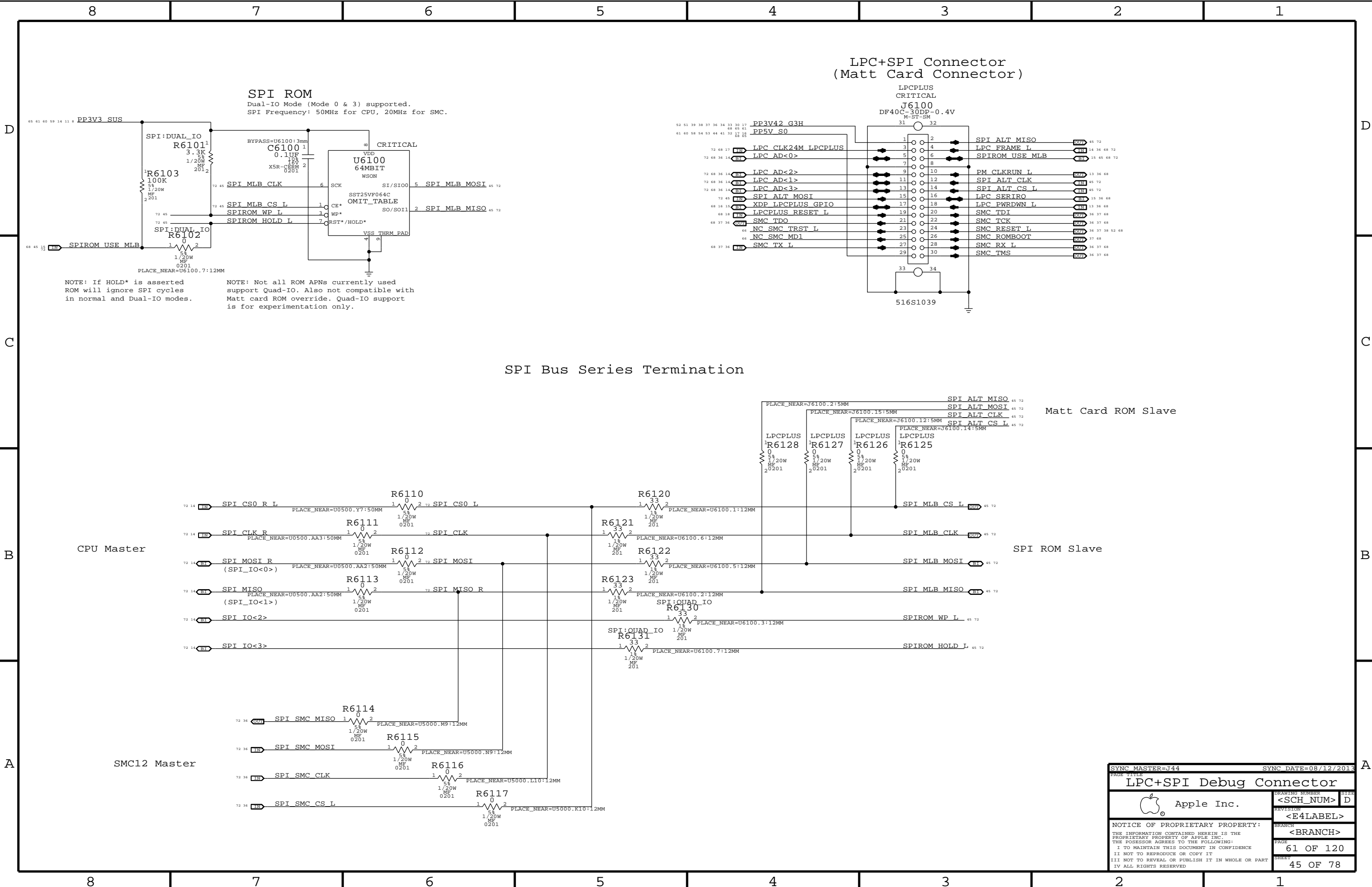


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D

C

A



SPI ROM

Dual-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.

LPC+SPI Connector
(Matt Card Connector)

LPCPLUS
CRITICAL
J6100
DF40C-30DP-0.4V
M-ST-SW


SPI Bus Series Termination

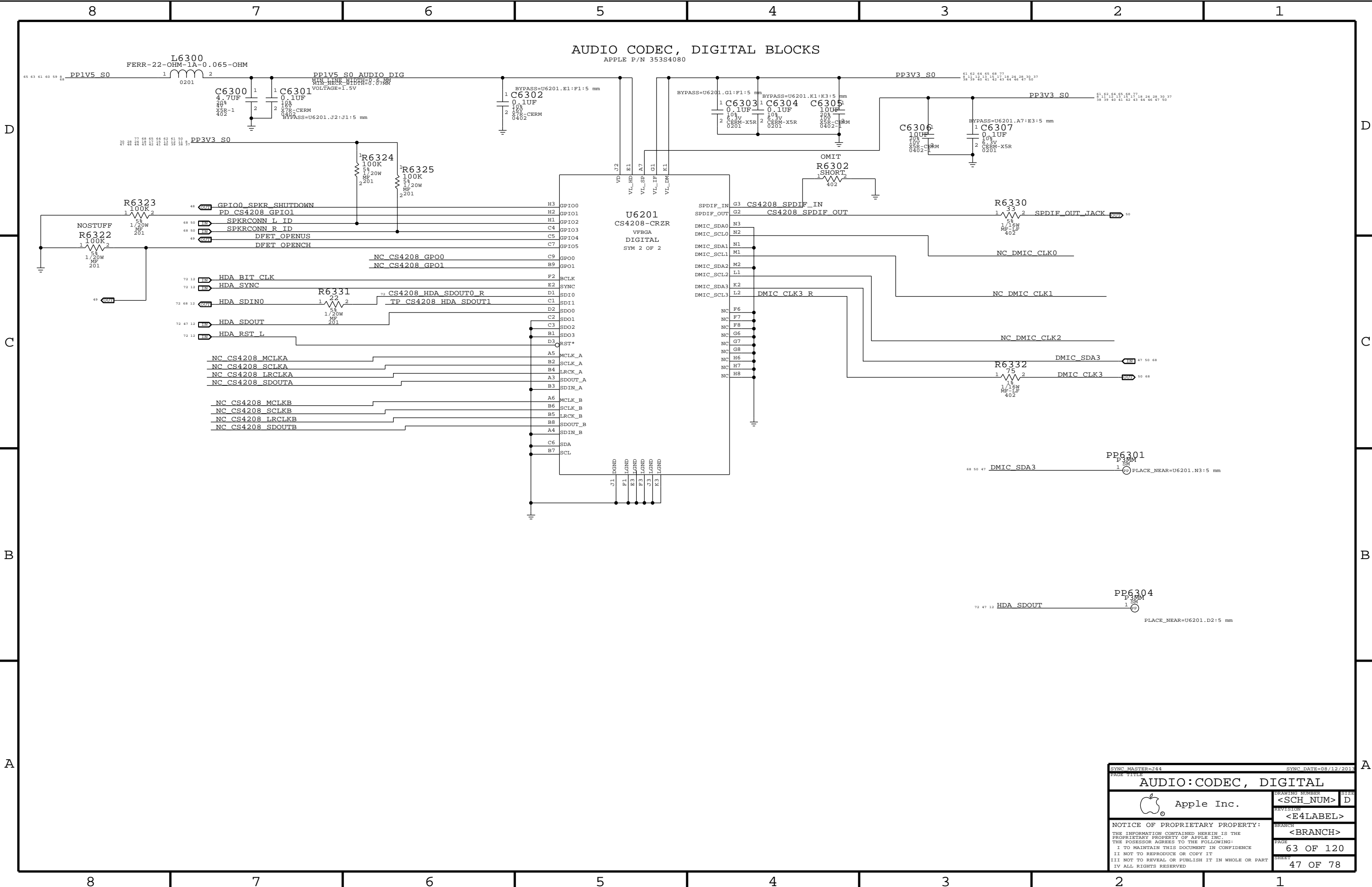
Matt Card ROM Slave

SPI ROM Slave

CPU Master

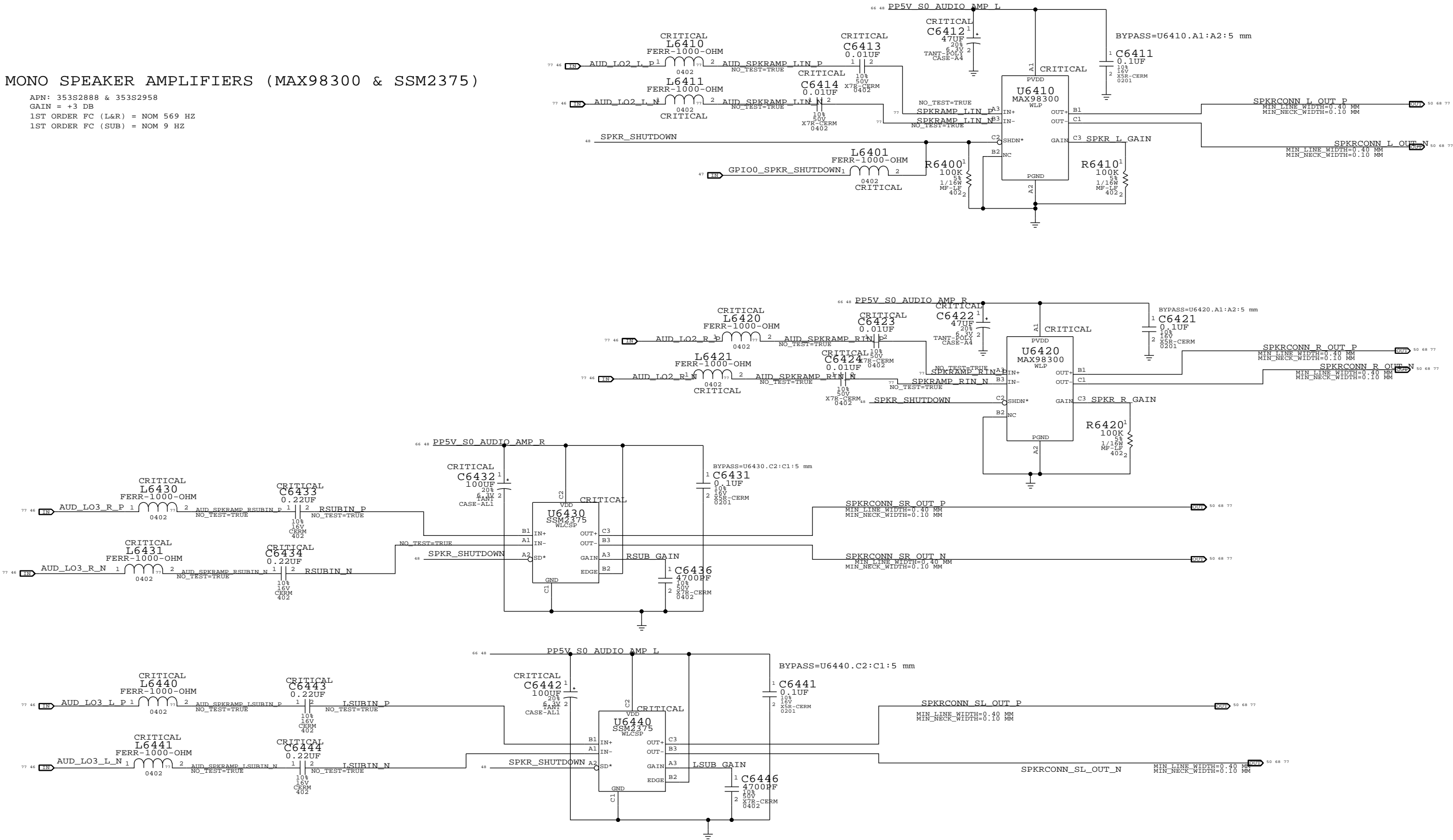
SMC12 Master


SYNC MASTER=J44		SYNC DATE=08/12/2013	
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LPC+SPI Debug Connector			
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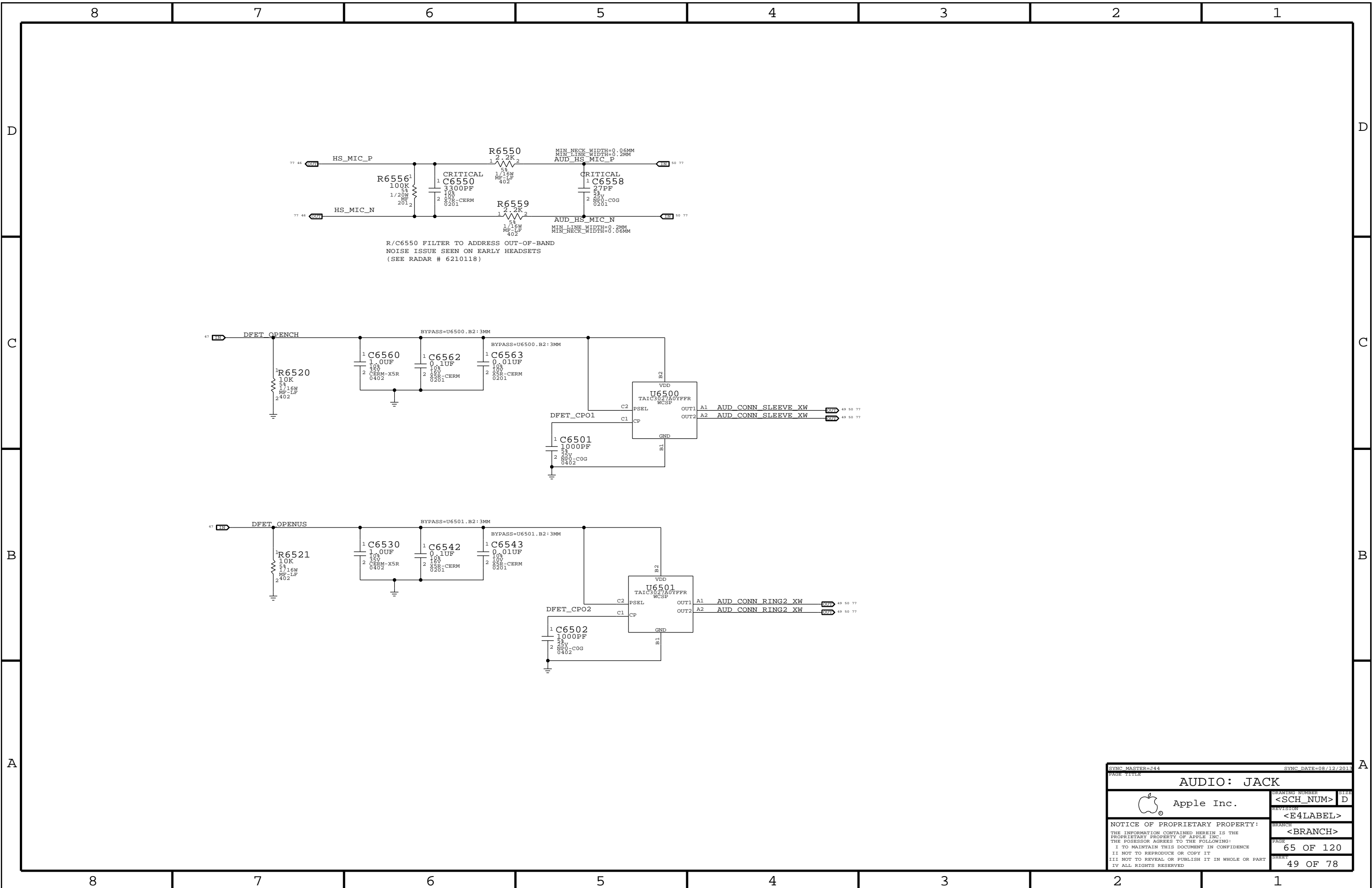


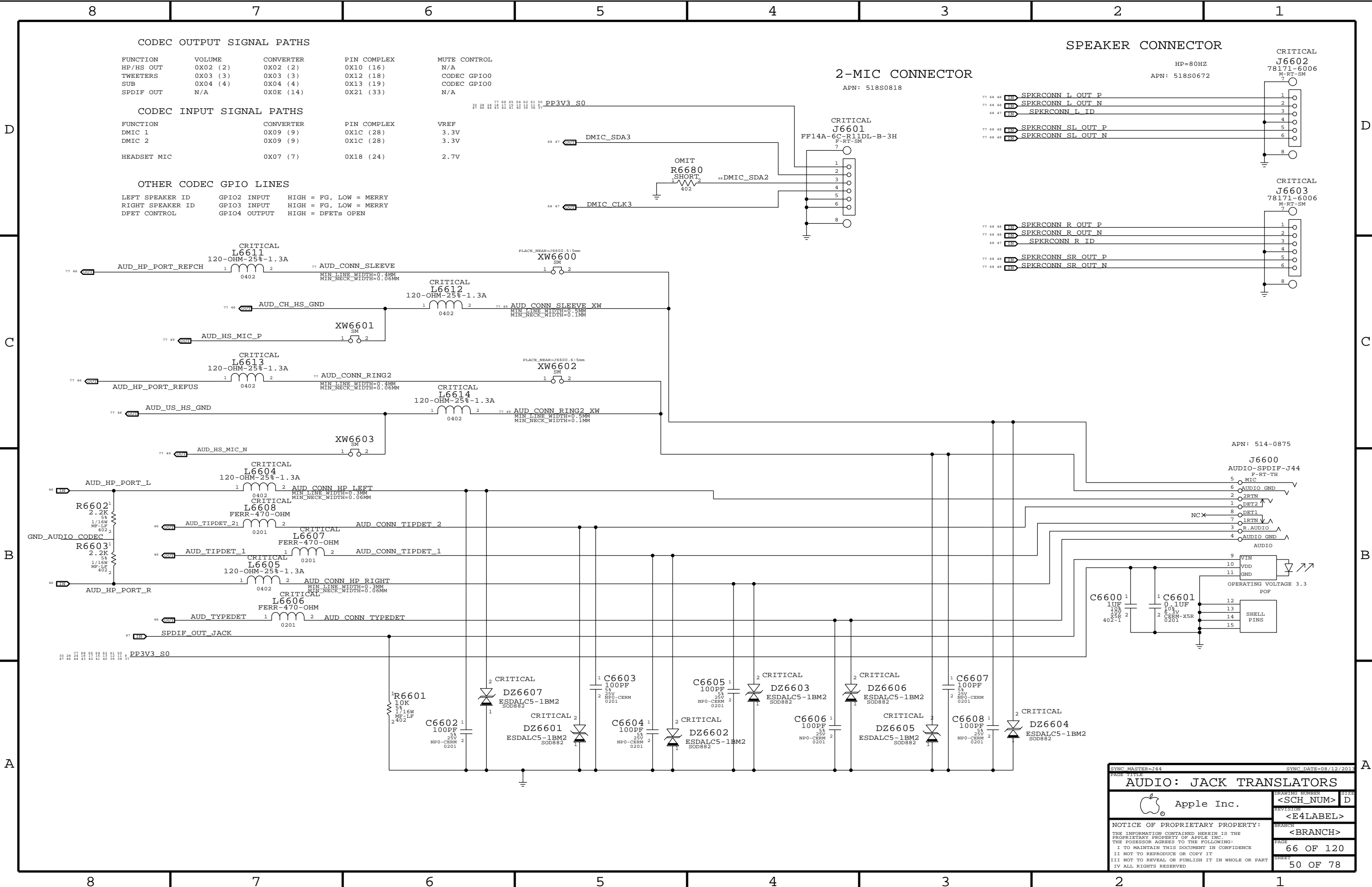
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)

APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=J44		SYNC DATE=08/12/2013	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETS OPEN

SPEAKER CONNECTOR

HP=80HZ
APN: 518S0672

2-MIC CONNECTOR

APN: 518S0818

CRITICAL
J6602
78171-6006
M-RT-SM

CRITICAL
J6603
78171-6006
M-RT-SM

APN: 514-0875

J6600

AUDIO-SPDIF-J44

F-RT-TH

5 MIC

6 AUDIO GND

2 2RTN

1 DET2

8 DET1

7 1RTN

3 R.AUDIO

4 AUDIO GND

AUDIO

9 VIN

10 VDD

11 GND

OPERATING VOLTAGE 3.3

POF

12 SHELL

13 PINS

14

15

SYNC MASTER=J44

SYNC DATE=08/12/2013

AUDIO: JACK TRANSLATORS

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<SCH_NUM>

REVISION

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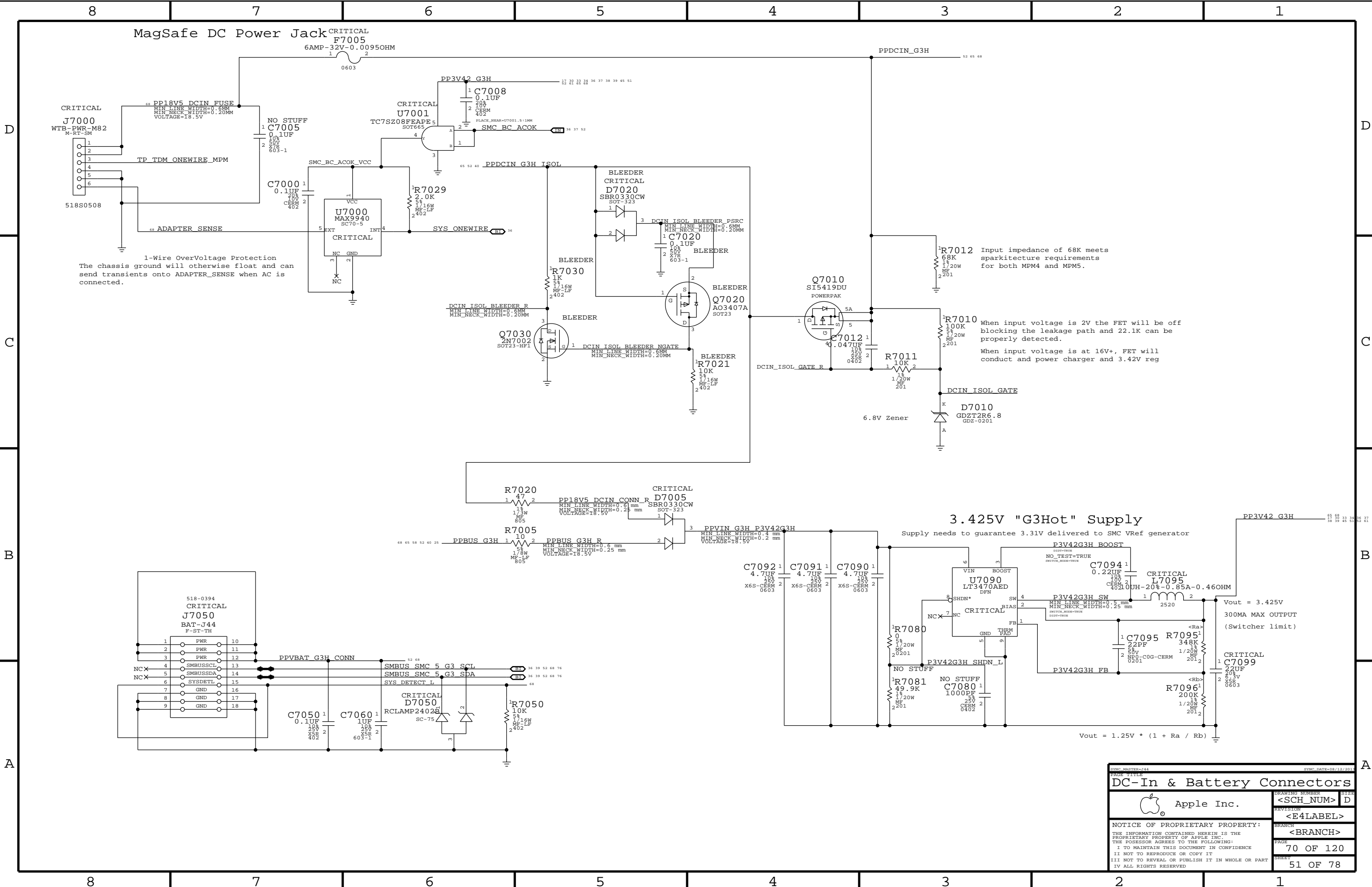
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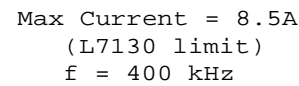
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SHEET

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Inrush Limiter



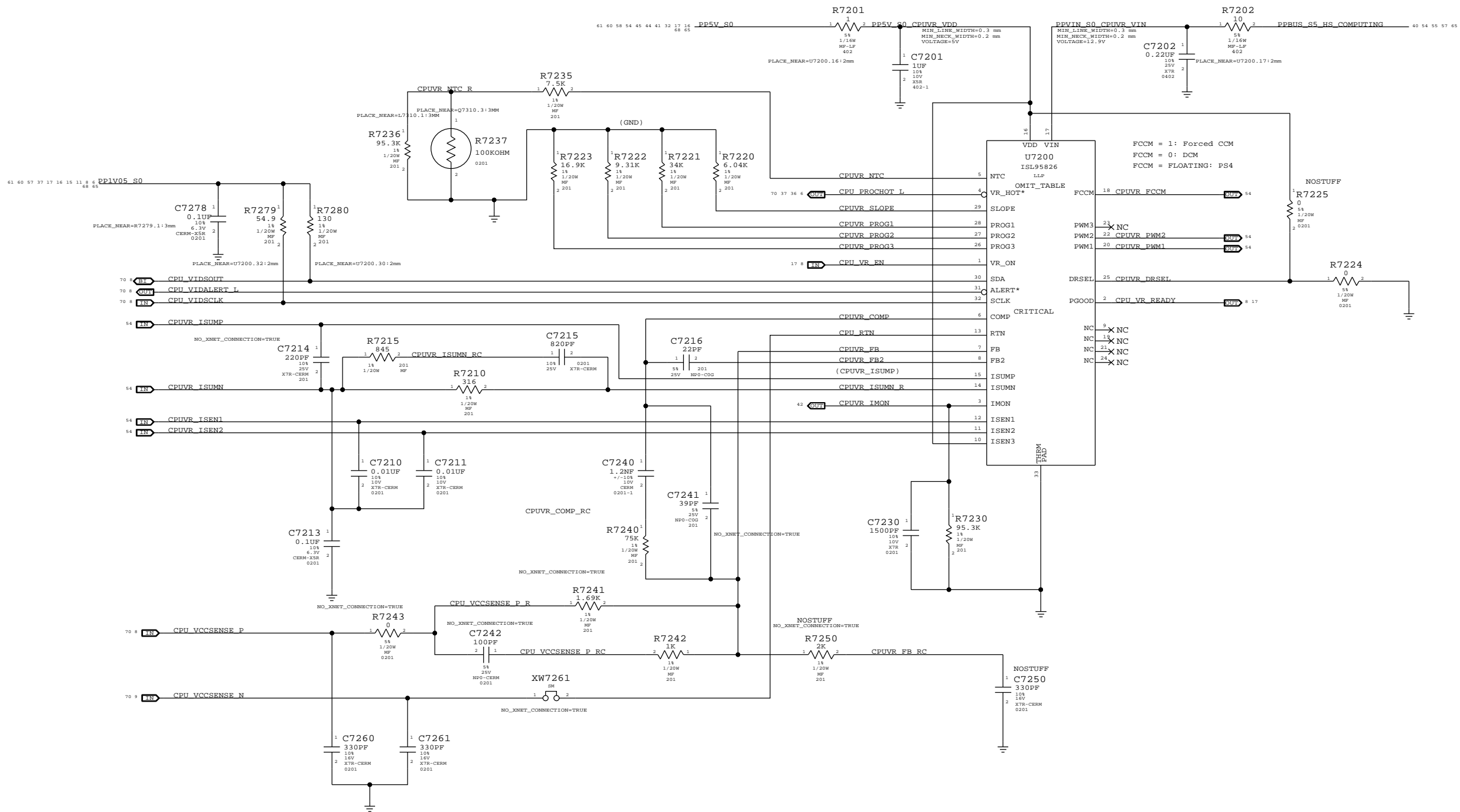
Vout = 5.50V
250MA MAX OUTPUT
(Switcher limit)


$$V_{out} = 1.25V * (1 + R_a / R_b)$$

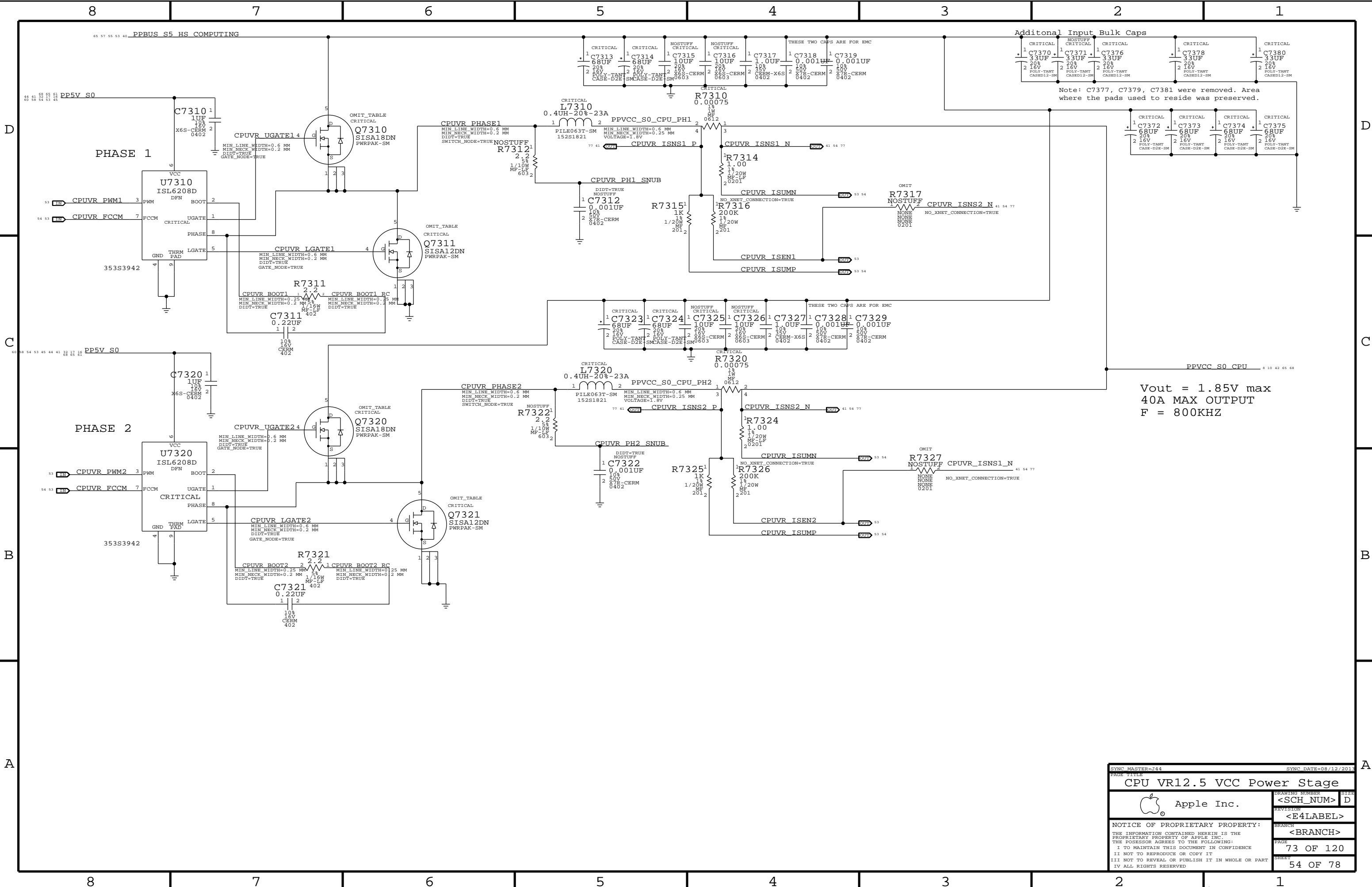
TO SYSTEM


TO/FROM BATTERY

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC, ISL95826R6200, PWM, PGOOD, SCREEN, 32P, QFN	U7200	CRITICAL	

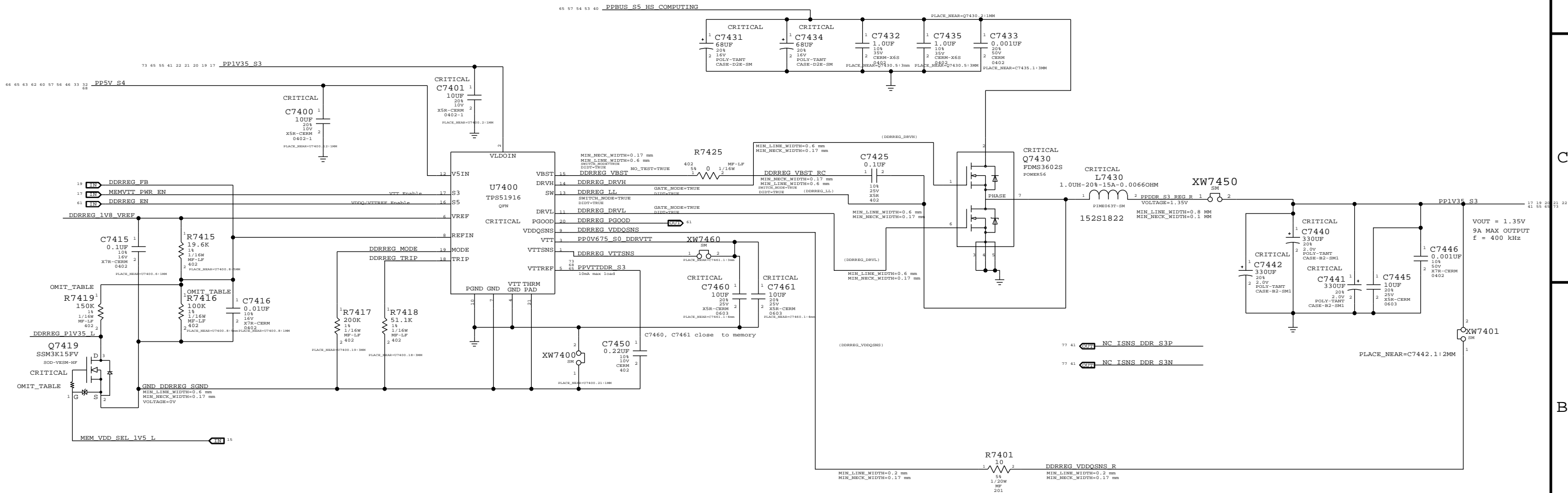


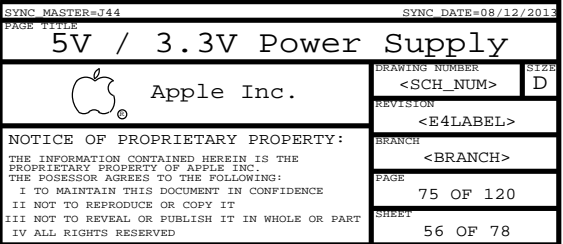
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PAGE TITLE			
CPU VR12.6 VCC Regulator IC			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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PAGE TITLE			
CPU VR12.5 VCC Power Stage			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		<BRANCH>	
		PAGE	73 OF 120
		SHEET	54 OF 78

DDR3L (1V35 S3) REGULATOR





D

C

B

A

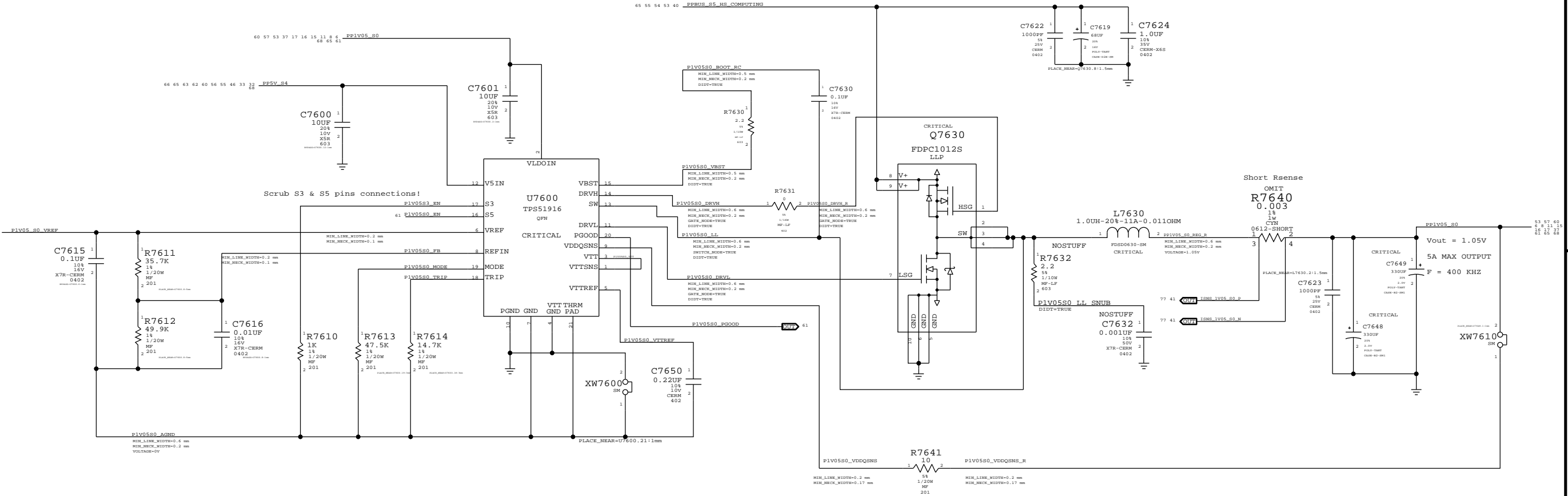
D


C

B

A

1.05V S0 Regulator



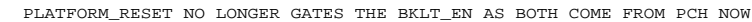
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1.05V S0 Power Supply			
 Apple Inc.		DRAWING NUMBER	SIZE
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		<BRANCH>	
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```
Power aliases required by this page:

--PP1VIN_S0SM_LCDBELTFTET      (9-12.6V LCD BACKLIGHT INPUT)
--PP5V_S0_RSLT                  (5V BACKLIGHT DRIVER INPUT)
--PP5V_S0SM_ENKLED              (5V KEYBOARD BACKLIGHT INPUT)
```

BOM options provided by this page:

```
BLT1:SRC - Stuffs 10.2 ohm series R for engineering builds
BLT1:PROC - Stuffs 0 ohm series R for production
```



```

KBDLED_CATHODE1      35 68
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM

100M

KBDLED_CATHODE2      35 68
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM

```

SANDWICH C7720 AND C7721
PLACE_NEAR=L7720.1:5MM PLACE_NEAR=L7720.1:5MM PLACE_NEAR=L7720.1:5MM

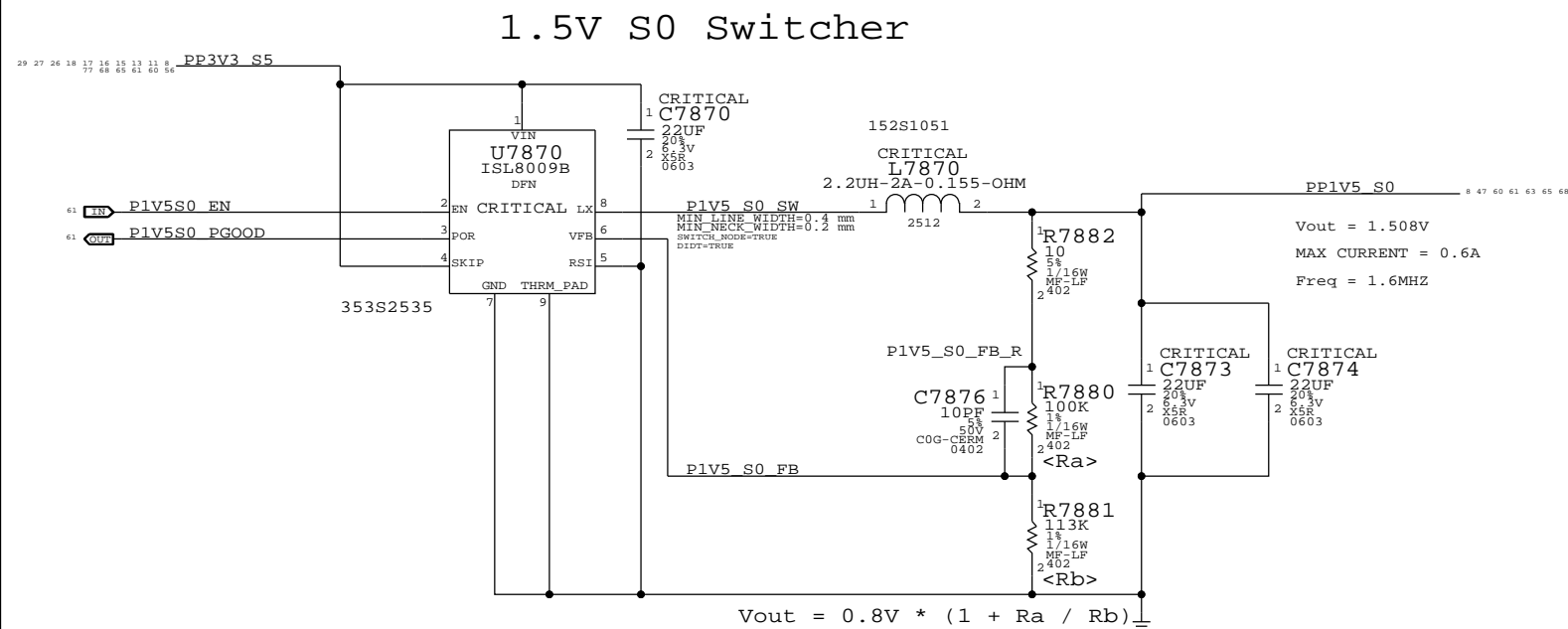
SANDWICH C7723 AND C7724

KBD BKLT LINE WIDTHS

PP5V S0 BKLT D 58
MIN_LINE_WIDTH=2 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V

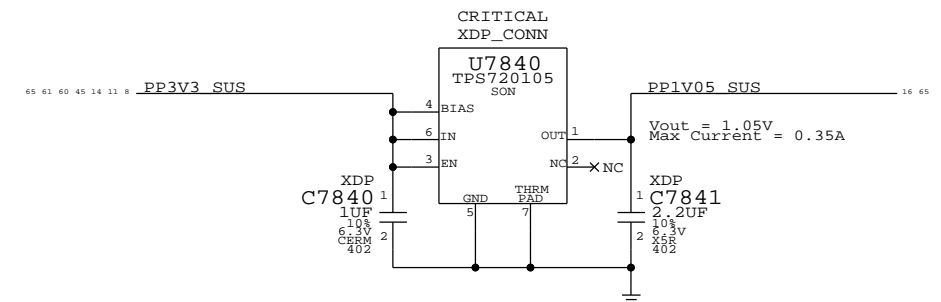
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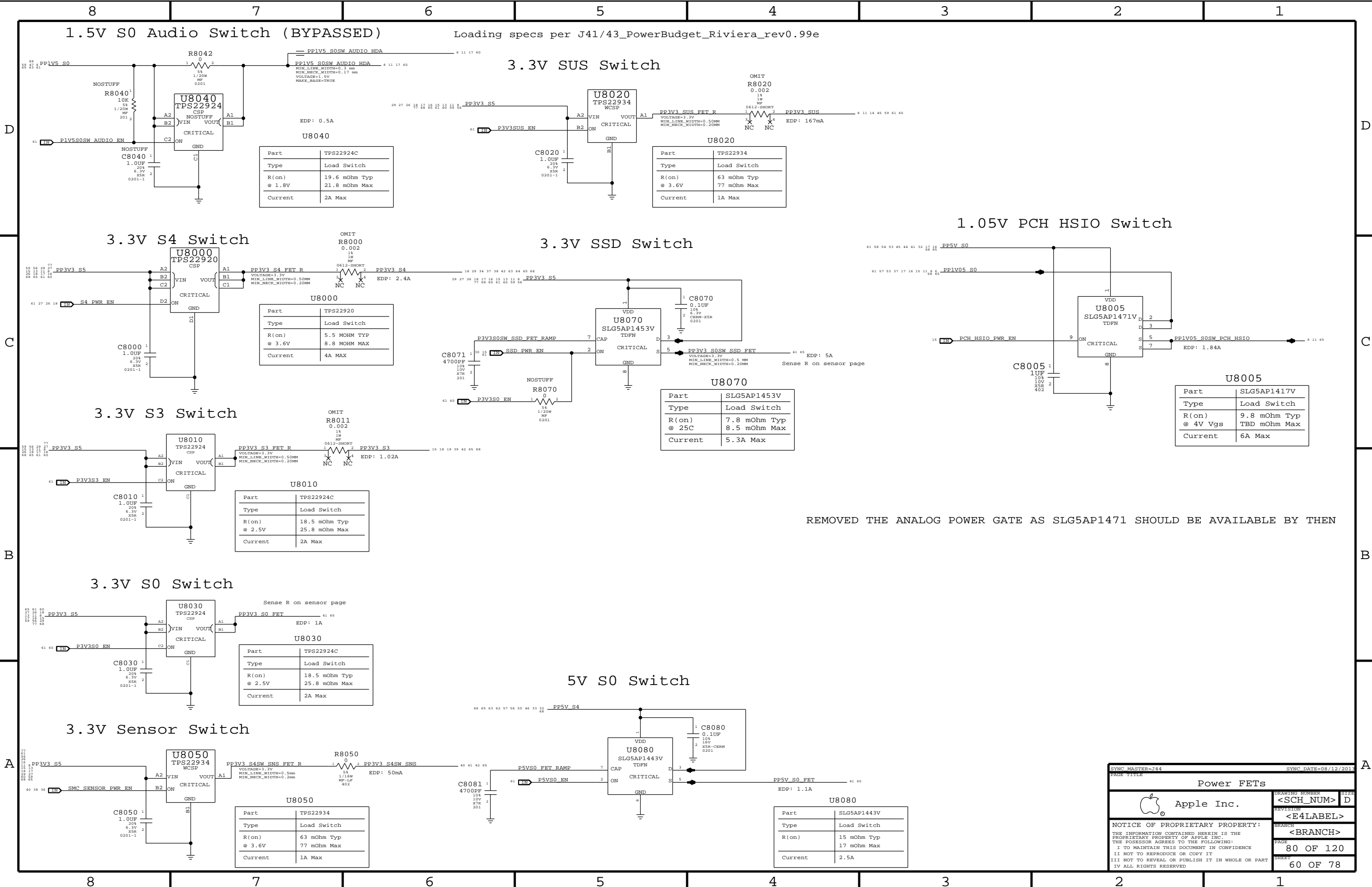
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1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.





Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

1.5V S0 Audio Switch (BYPASSED)

3.3V SUS Switch

1.05V PCH HSIO Switch

3.3V S4 Switch

3.3V SSD Switch

3.3V S3 Switch

3.3V S0 Switch

3.3V Sensor Switch


5V S0 Switch

REMOVED THE ANALOG POWER GATE AS SLG5AP1471 SHOULD BE AVAILABLE BY THEN

SYNC MASTER=J44

SYNC DATE=08/12/2013

Power FETs

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DRAWING NUMBER<SCH_NUM>D

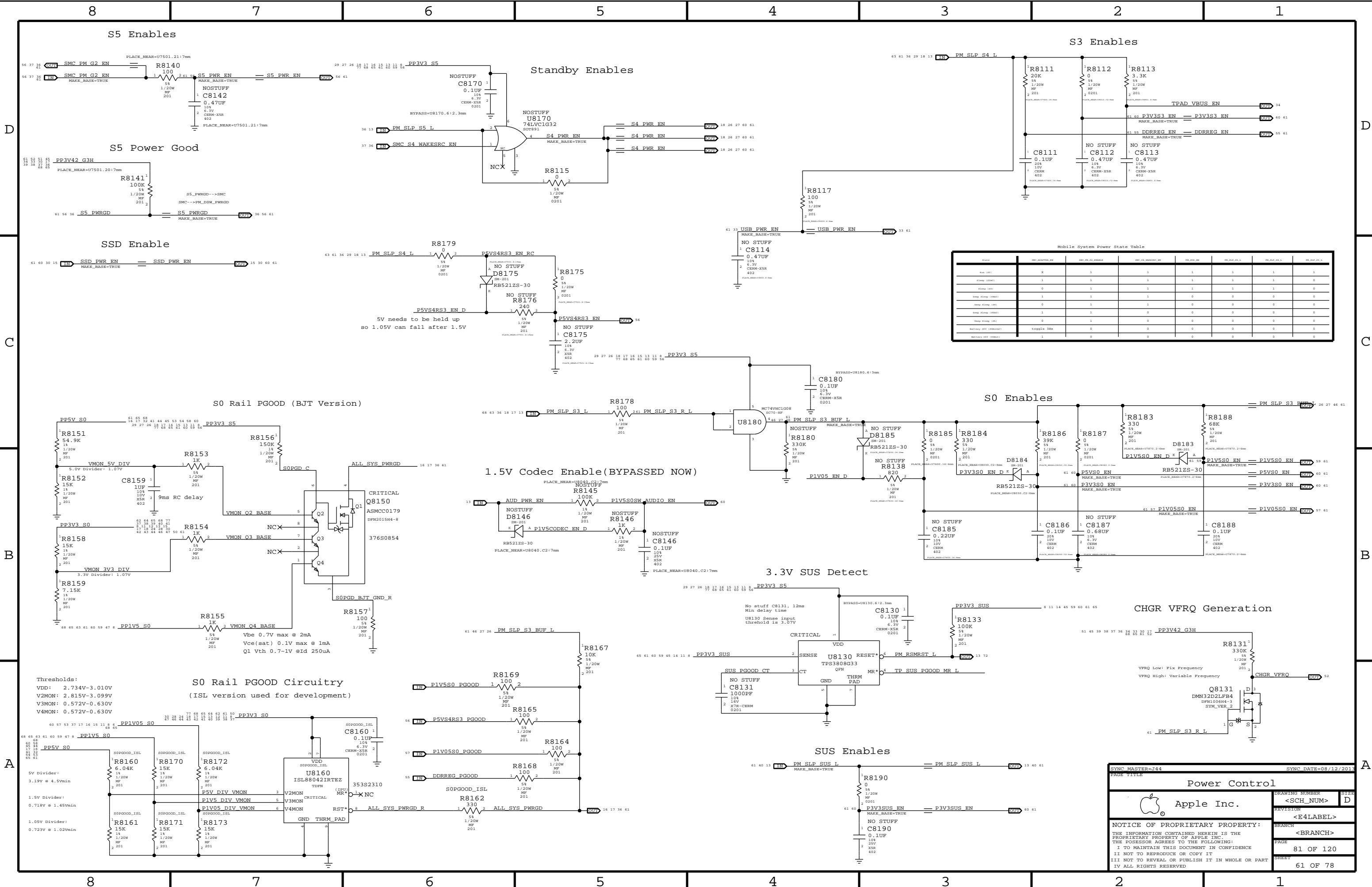
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Mobile System Power State Table

State	SMC_DISABLE_EN	SMC_P3V3_DISABLE	SMC_P5V5_DISABLE	PM_P3V3_EN	PM_P5V5_EN	PM_P3V3_L	PM_P5V5_L
Run (R0)	1	1	1	1	1	1	1
Standby (S0)	1	1	1	1	1	1	0
Deep Standby (S1)	1	1	1	0	0	0	0
Deep Standby (S2)	0	1	1	0	0	0	0
Deep Standby (S3)	1	1	1	0	0	0	0
Deep Standby (S4)	1	1	0	0	0	0	0
Battery off (S5)	0	0	0	0	0	0	0
Battery off (S6)	1	0	0	0	0	0	0
Battery off (S7)	1	0	0	0	0	0	0

SYNC MASTER=144

SYNC DATE=08/12/2013

Power Control

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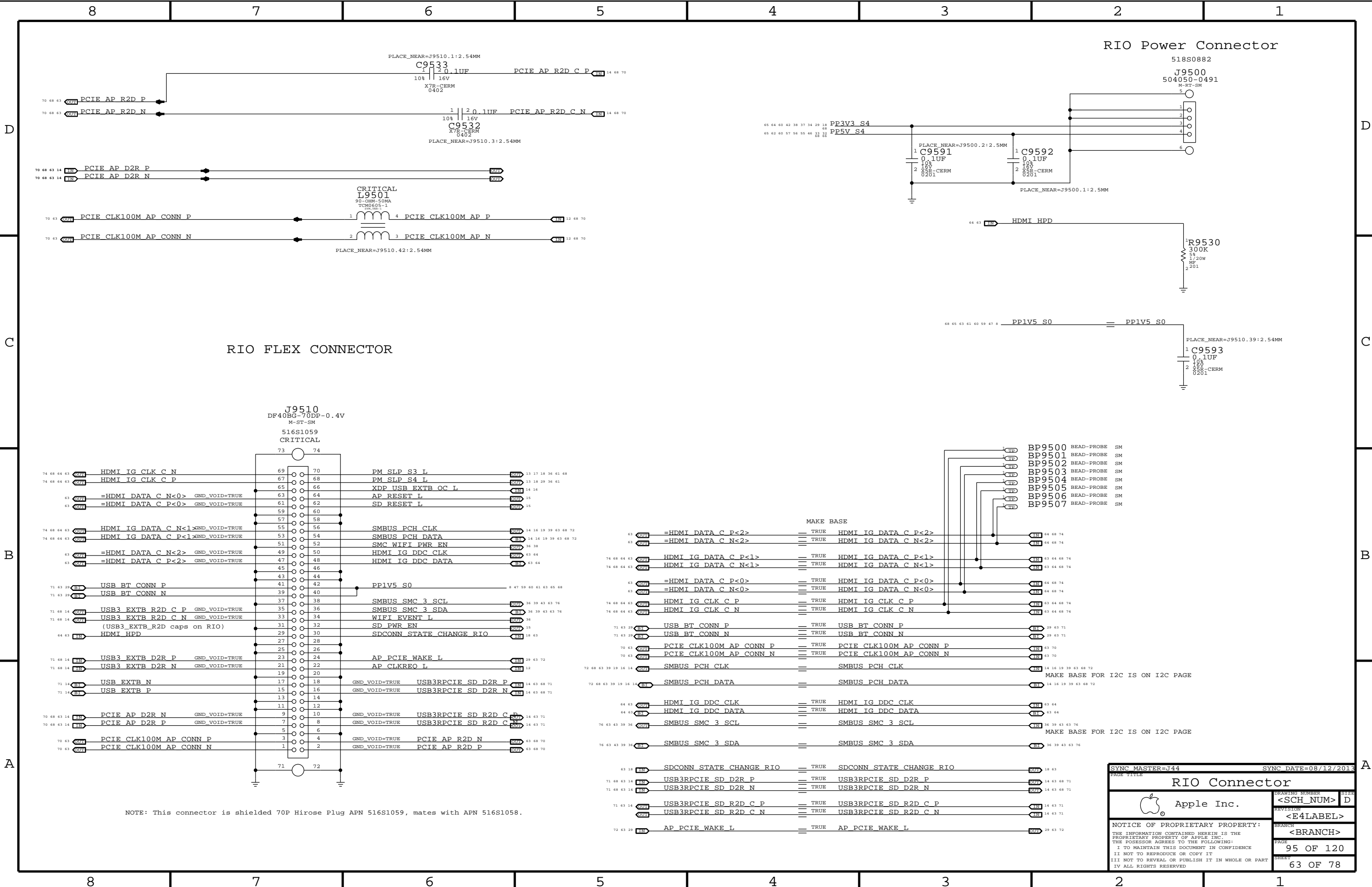
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<SCH_NUM>

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<BRANCH>

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RIO Power Connector

518S0882

J9500

504050-0491

M-RT-SM

5

1

2

3

4

6

1

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9500.2:2.5MM

1

0.1UF

PLACE_NEAR=J9500.1:2.5MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.39:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.1:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.2:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.3:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.4:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.5:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.6:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.7:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.8:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.9:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.10:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.11:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.12:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.13:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.14:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.15:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.16:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.17:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.18:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.19:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.20:2.54MM

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100

16V

X7R-CERM

0201

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100

16V

X7R-CERM

0201

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100

16V

X7R-CERM

0201

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0.1UF

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100

16V

X7R-CERM

0201

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0.1UF

PLACE_NEAR=J9510.24:2.54MM

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100

16V

X7R-CERM

0201

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0.1UF

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100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.26:2.54MM

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16V

X7R-CERM

0201

1

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PLACE_NEAR=J9510.27:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.28:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.29:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.30:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.31:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.32:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.33:2.54MM

2

100

16V

X7R-CERM

0201

1

0.1UF

PLACE_NEAR=J9510.34:2.54MM

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0.1UF

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2

100

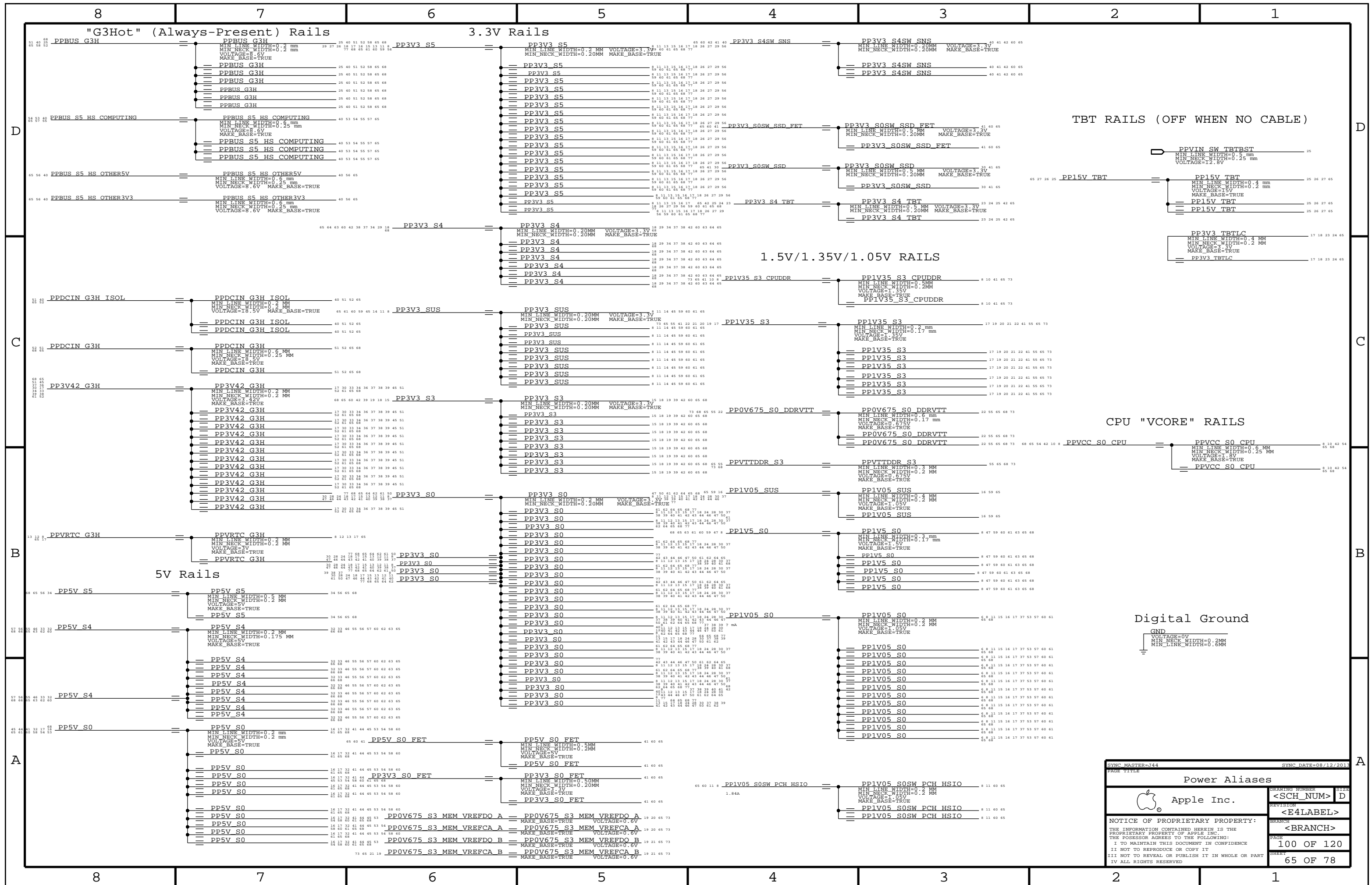
16V

X7R-CERM


0201

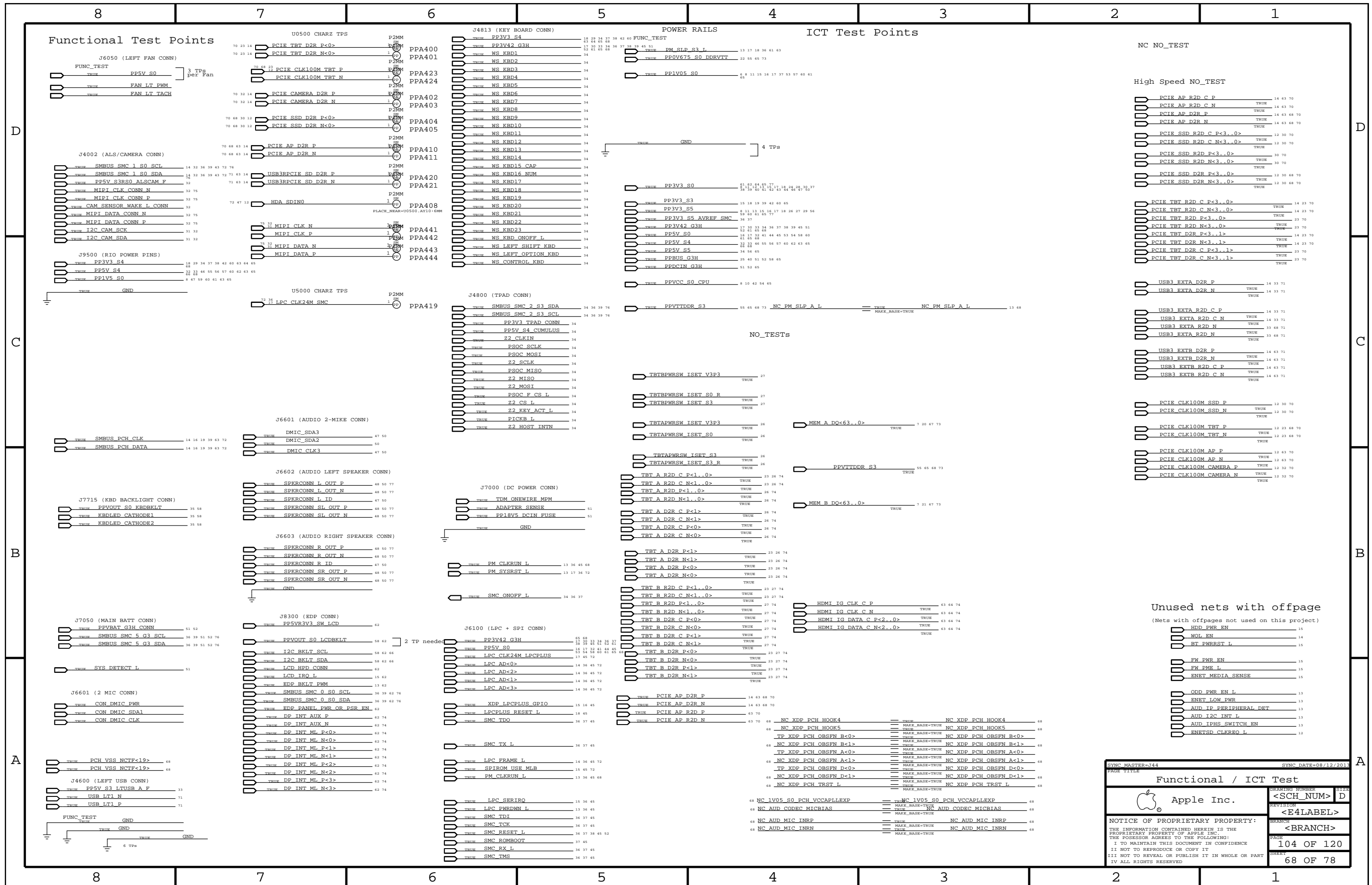
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0.1UF



8	7	6	5	4	3	2	1
Memory Bit/Byte Swizzle							
MAKE_BASE							
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73 68 7	TRUE	MEM A DQ<1>	=	MEM A DQ<56>	20		
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73 68 7	TRUE	MEM A DQ<7>	=	MEM A DQ<63>	20		
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73 68 7	TRUE	MEM A DQ<10>	=	MEM A DQ<45>	20		
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73 68 7	TRUE	MEM A DQ<20>	=	MEM A DQ<17>	20		
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73 68 67 20 7	TRUE	MEM A DQ<32>	=	MEM A DQ<32>	7 20 67 68 73		
73 68 7	TRUE	MEM A DQ<33>	=	MEM A DQ<24>	20		
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73 68 7	TRUE	MEM A DQ<38>	=	MEM A DQ<31>	20		
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73 68 7	TRUE	MEM A DQ<45>	=	MEM A DQ<10>	20		
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73 7	TRUE	MEM A DQS P<2>	=	MEM A DQS P<2>	20		
73 7	TRUE	MEM A DQS N<2>	=	MEM A DQS N<2>	20		
73 7	TRUE	MEM A DQS P<3>	=	MEM A DQS P<4>	20		
73 7	TRUE	MEM A DQS N<3>	=	MEM A DQS N<4>	20		
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73 7	TRUE	MEM A DQS N<5>	=	MEM A DQS N<1>	20		
73 67 20 7	TRUE	MEM A DQS P<6>	=	MEM A DQS P<6>	7 20 67 73		
73 67 20 7	TRUE	MEM A DQS N<6>	=	MEM A DQS N<6>	7 20 67 73		
73 7	TRUE	MEM A DQS P<7>	=	MEM A DQS P<0>	20		
73 7	TRUE	MEM A DQS N<7>	=	MEM A DQS N<0>	20		
MAKE_BASE							
73 68 7	TRUE	MEM B DQ<0>	=	MEM B DQ<8>	21		
73 68 7	TRUE	MEM B DQ<1>	=	MEM B DQ<14>	21		
73 68 7	TRUE	MEM B DQ<2>	=	MEM B DQ<11>	21		
73 68 7	TRUE	MEM B DQ<3>	=	MEM B DQ<9>	21		
73 68 7	TRUE	MEM B DQ<4>	=	MEM B DQ<12>	21		
73 68 7	TRUE	MEM B DQ<5>	=	MEM B DQ<10>	21		
73 68 7	TRUE	MEM B DQ<6>	=	MEM B DQ<15>	21		
73 68 7	TRUE	MEM B DQ<7>	=	MEM B DQ<13>	21		
73 68 7	TRUE	MEM B DQ<8>	=	MEM B DQ<24>	21		
73 68 7	TRUE	MEM B DQ<9>	=	MEM B DQ<30>	21		
73 68 7	TRUE	MEM B DQ<10>	=	MEM B DQ<29>	21		
73 68 7	TRUE	MEM B DQ<11>	=	MEM B DQ<27>	21		
73 68 7	TRUE	MEM B DQ<12>	=	MEM B DQ<28>	21		
73 68 7	TRUE	MEM B DQ<13>	=	MEM B DQ<26>	21		
73 68 7	TRUE	MEM B DQ<14>	=	MEM B DQ<25>	21		
73 68 7	TRUE	MEM B DQ<15>	=	MEM B DQ<31>	21		
73 68 7	TRUE	MEM B DQ<16>	=	MEM B DQ<5>	21		
73 68 7	TRUE	MEM B DQ<17>	=	MEM B DQ<1>	21		
73 68 7	TRUE	MEM B DQ<18>	=	MEM B DQ<6>	21		
73 68 7	TRUE	MEM B DQ<19>	=	MEM B DQ<3>	21		
73 68 7	TRUE	MEM B DQ<20>	=	MEM B DQ<4>	21		
73 68 7	TRUE	MEM B DQ<21>	=	MEM B DQ<7>	21		
73 68 7	TRUE	MEM B DQ<22>	=	MEM B DQ<0>	21		
73 68 7	TRUE	MEM B DQ<23>	=	MEM B DQ<2>	21		
73 68 7	TRUE	MEM B DQ<24>	=	MEM B DQ<21>	21		
73 68 7	TRUE	MEM B DQ<25>	=	MEM B DQ<17>	21		
73 68 7	TRUE	MEM B DQ<26>	=	MEM B DQ<20>	21		
73 68 7	TRUE	MEM B DQ<27>	=	MEM B DQ<22>	21		
73 68 7	TRUE	MEM B DQ<28>	=	MEM B DQ<23>	21		
73 68 7	TRUE	MEM B DQ<29>	=	MEM B DQ<19>	21		
73 68 7	TRUE	MEM B DQ<30>	=	MEM B DQ<18>	21		
73 68 7	TRUE	MEM B DQ<31>	=	MEM B DQ<16>	21		
73 68 67 21 7	TRUE	MEM B DQ<32>	=	MEM B DQ<32>	7 21 67 68 73		
73 68 7	TRUE	MEM B DQ<33>	=	MEM B DQ<40>	21		
73 68 7	TRUE	MEM B DQ<34>	=	MEM B DQ<45>	21		
73 68 7	TRUE	MEM B DQ<35>	=	MEM B DQ<43>	21		
73 68 7	TRUE	MEM B DQ<36>	=	MEM B DQ<46>	21		
73 68 7	TRUE	MEM B DQ<37>	=	MEM B DQ<42>	21		
73 68 7	TRUE	MEM B DQ<38>	=	MEM B DQ<47>	21		
73 68 7	TRUE	MEM B DQ<39>	=	MEM B DQ<41>	21		
73 68 7	TRUE	MEM B DQ<40>	=	MEM B DQ<60>	21		
73 68 7	TRUE	MEM B DQ<41>	=	MEM B DQ<56>	21		
73 68 7	TRUE	MEM B DQ<42>	=	MEM B DQ<63>	21		
73 68 7	TRUE	MEM B DQ<43>	=	MEM B DQ<61>	21		
73 68 7	TRUE	MEM B DQ<44>	=	MEM B DQ<62>	21		
73 68 7	TRUE	MEM B DQ<45>	=	MEM B DQ<58>	21		
73 68 7	TRUE	MEM B DQ<46>	=	MEM B DQ<59>	21		
73 68 7	TRUE	MEM B DQ<47>	=	MEM B DQ<57>	21		
73 68 7	TRUE	MEM B DQ<48>	=	MEM B DQ<38>	21		
73 68 7	TRUE	MEM B DQ<49>	=	MEM B DQ<37>	21		
73 68 7	TRUE	MEM B DQ<50>	=	MEM B DQ<32>	21		
73 68 7	TRUE	MEM B DQ<51>	=	MEM B DQ<33>	21		
73 68 7	TRUE	MEM B DQ<52>	=	MEM B DQ<35>	21		
73 68 7	TRUE	MEM B DQ<53>	=	MEM B DQ<36>	21		
73 68 7	TRUE	MEM B DQ<54>	=	MEM B DQ<34>	21		
73 68 7	TRUE	MEM B DQ<55>	=	MEM B DQ<39>	21		
73 68 7	TRUE	MEM B DQ<56>	=	MEM B DQ<51>	21		
73 68 7	TRUE	MEM B DQ<57>	=	MEM B DQ<53>	21		
73 68 7	TRUE	MEM B DQ<58>	=	MEM B DQ<48>	21		
73 68 7	TRUE	MEM B DQ<59>	=	MEM B DQ<55>	21		
73 68 7	TRUE	MEM B DQ<60>	=	MEM B DQ<50>	21		
73 68 7	TRUE	MEM B DQ<61>	=	MEM B DQ<49>	21		
73 68 7	TRUE	MEM B DQ<62>	=	MEM B DQ<54>	21		
73 68 7	TRUE	MEM B DQ<63>	=	MEM B DQ<52>	21		
73 7	TRUE	MEM B DQS P<0>	=	MEM B DQS P<1>	21		
73 7	TRUE	MEM B DQS N<0>	=	MEM B DQS N<1>	21		
73 7	TRUE	MEM B DQS P<1>	=	MEM B DQS P<3>	21		
73 7	TRUE	MEM B DQS N<1>	=	MEM B DQS N<3>	21		
73 7	TRUE	MEM B DQS P<2>	=	MEM B DQS P<0>	21		
73 7	TRUE	MEM B DQS N<2>	=	MEM B DQS N<0>	21		
73 7	TRUE	MEM B DQS P<3>	=	MEM B DQS P<2>	21		
73 7	TRUE	MEM B DQS N<3>	=	MEM B DQS N<2>	21		
73 7	TRUE	MEM B DQS P<4>	=	MEM B DQS P<5>	21		
73 7	TRUE	MEM B DQS N<4>	=	MEM B DQS N<5>	21		
73 7	TRUE	MEM B DQS P<5>	=	MEM B DQS P<7>	21		
73 7	TRUE	MEM B DQS N<5>	=	MEM B DQS N<7>	21		
73 67 21 7	TRUE	MEM B DQS P<6>	=	MEM B DQS P<6>	7 21 67 73		
73 67 21 7	TRUE	MEM B DQS N<6>	=	MEM B DQS N<6>	7 21 67 73		
73 7	TRUE	MEM B DQS P<7>	=	MEM B DQS P<6>	21		
73 7	TRUE	MEM B DQS N<7>	=	MEM B DQS N<6>	21		

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Memory Bit/Byte Swizzle			
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J44 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA, P65BGA, BGA_MEM	MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?


Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	.	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1x_DIELECTRIC	1SL3, 1SL4, 1SL9, 1SL10	0.053 MM	?
1X_DIELECTRIC	1SL2, 1SL5, 1SL6, 1SL7, 1SL8, 1SL11	0.101 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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PCB Rule Definitions			
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_08MIL	*	0.203 MM	?
CPU_12MIL	*	0.305 MM	?
CPU_18MIL	*	0.457 MM	?
CPU_25MIL	*	0.635 MM	?

PCI Express Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?















































SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

CPU Signal Properties

ELECTRICAL CONSTRAINT SET		NET TYPE			
		PHYSICAL	SPACING		
□	XDP_TCK0	CPU_45S	CPU_18MTL	XDP_CPU_TCK	6 16
□	XDP_TCK0	CPU_45S	CPU_18MTL	PCH_JTAGX	12 16
□	XDP_TCK1	CPU_45S	CPU_18MTL	XDP_PCH_TCK	12 16
□	XDP_TDO	CPU_45S		XDP_CPU_TDO	6 16
□	XDP_TDO	CPU_45S		XDP_PCH_TDO	12 16
□	XDP_TDI	CPU_45S		XDP_CPU_TDI	6 16
□	XDP_TDI	CPU_45S		XDP_PCH_TDI	12 16
□	XDP_TMS	CPU_45S		XDP_CPU_TMS	6 16
□	XDP_TMS	CPU_45S		XDP_PCH_TMS	12 16
□	XDP_TRST_L	CPU_45S		XDP_TRST_L	16
□	XDP_TRST_L	CPU_45S		XDP_CPU_PCH_TRST_L	6 12 16
□	XDP_PRDY_L	CPU_45S		XDP_CPU_PRDY_L	6 16
□	XDP_PREQ_L	CPU_45S		XDP_CPU_PREQ_L	6 16
□	CPU_VCCST_PWRGD	CPU_45S	CPU_08MTL	CPU_VCCST_PWRGD	8 16 17
□	CPU_VCCST_PWRGD	CPU_45S	CPU_08MTL	XDP_CPU_VCCST_PWRGD	16
□	CPU_BEM	CPU_45S	CPU_08MTL	XDP_BPM_L<1..0>	6 16
□	CPU_BEM_TP	CPU_45S		XDP_BPM_L<7..2>	6 16
□	CPU_RCOMP_SM	CPU_27P4S	CPU_25MTL	CPU_SM_RCOMP<2..0>	6
□	CPU_RCOMP_EDP	CPU_27P4S	CPU_25MTL	MCP_EDP_RCOMP	6
□	CPU_RCOMP_OPI	CPU_27P4S	CPU_12MTL	CPU_OPI_RCOMP	6
□	CPU_PROCHOT	CPU_45S	CPU_08MTL	CPU_PROCHOT_L	6 16 37 53
□	CPU_PROCHOT	CPU_45S	CPU_08MTL	CPU_PROCHOT_R_L	6
□	CPU_CATERR	CPU_45S	CPU_08MTL	CPU_CATERR_L	6 16
□	CPU_VIDALERT	CPU_45S	CPU_18MTL	CPU_VIDALERT_L	8 53
□	CPU_VIDALERT	CPU_45S	CPU_18MTL	CPU_VIDALERT_R_L	8
□	CPU_VIDSCLK	CPU_45S	CPU_18MTL	CPU_VIDSCLK	8 53
□	CPU_VIDSCLK	CPU_45S	CPU_18MTL	CPU_VIDSCLK_R	8
□	CPU_VIDSOUT	CPU_45S	CPU_18MTL	CPU_VIDSOUT	8 53
□	CPU_VIDSOUT	CPU_45S	CPU_18MTL	CPU_VIDSOUT_R	8
□	CPU_PECI	CPU_45S	CPU_18MTL	CPU_PECI	6 37
□	CPU_PECI	CPU_45S	CPU_18MTL	CPU_PECI_R	16 37
□	CPU_PECI_SMC	CPU_45S	CPU_18MTL	SMC_PECI_L	16 37
□	CPU_PECI_SMC	CPU_45S	CPU_18MTL	SMC_PECI_L_R	37
□	CPU_CFG	CPU_45S		CPU_CFG<19..11>	6 16
□	CPU_CFG_PD	CPU_45S		CPU_CFG<10..8>	6 16
□	CPU_CFG	CPU_45S		CPU_CFG<7..5>	6 16
□	CPU_CFG_PD	CPU_45S		CPU_CFG<4>	6 16
□	CPU_CFG_3	CPU_45S		CPU_CFG<3>	6 16
□	CPU_CFG	CPU_45S		CPU_CFG<2>	6 16
□	CPU_CFG_PD	CPU_45S		CPU_CFG<1..0>	6 16
□	CPU_MEM_RESET	CPU_45S	CPU_08MTL	MEM_RESET_L	20 21 22
□	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 53
□	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 53

PCI Express Properties

ELECTRICAL CONST SET		NET TYPE			
		PHYSICAL	SPACING		
	PCIE SSD D2R	PCIE_85D	PCIE_RY	PCIE SSD D2R P<3..1>	12 30 68
	PCIE SSD D2R	PCIE_85D	PCIE_RY	PCIE SSD D2R N<3..1>	12 30 68
	PCIE SSD D2R_PP	PCIE_85D	PCIE_RY	PCIE SSD D2R P<0>	12 30 68
	PCIE SSD D2R_PP	PCIE_85D	PCIE_RY	PCIE SSD D2R N<0>	12 30 68
	PCIE SSD R2D	PCIE_85D	PCIE_TY	PCIE SSD R2D C P<3..0>	12 30 68
	PCIE SSD R2D	PCIE_85D	PCIE_TY	PCIE SSD R2D C N<3..0>	12 30 68
	PCIE SSD R2D	PCIE_85D	PCIE_TY	PCIE SSD R2D P<3..1>	30 68
	PCIE SSD R2D	PCIE_85D	PCIE_TY	PCIE SSD R2D N<3..0>	30 68
	PCIE TBT D2R_0	PCIE_85D	PCIE_RY	PCIE TBT D2R P<0>	14 23 68
	PCIE TBT D2R_0	PCIE_85D	PCIE_RY	PCIE TBT D2R N<0>	14 23 68
	PCIE TBT D2R_0	PCIE_85D	PCIE_RY	PCIE TBT D2R C P<0>	23
	PCIE TBT D2R_0	PCIE_85D	PCIE_RY	PCIE TBT D2R C N<0>	23
	PCIE TBT D2R	PCIE_85D	PCIE_RY	PCIE TBT D2R P<3..1>	14 23 68
	PCIE TBT D2R	PCIE_85D	PCIE_RY	PCIE TBT D2R N<3..1>	14 23 68
	PCIE TBT D2R	PCIE_85D	PCIE_RY	PCIE TBT D2R C P<3..1>	23 68
	PCIE TBT D2R	PCIE_85D	PCIE_RY	PCIE TBT D2R C N<3..1>	23 68
	PCIE TBT R2D	PCIE_85D	PCIE_TY	PCIE TBT R2D P<3..0>	23 68
	PCIE TBT R2D	PCIE_85D	PCIE_TY	PCIE TBT R2D N<3..0>	23 68
	PCIE TBT R2D	PCIE_85D	PCIE_TY	PCIE TBT R2D C P<3..0>	14 23 68
	PCIE TBT R2D	PCIE_85D	PCIE_TY	PCIE TBT R2D C N<3..0>	14 23 68
	PCIE AP R2D	PCIE_85D	PCIE_TY	PCIE AP R2D P	63 68
	PCIE AP R2D	PCIE_85D	PCIE_TY	PCIE AP R2D N	63 68
	PCIE AP R2D	PCIE_85D	PCIE_TY	PCIE AP R2D C P	14 63 68
	PCIE AP R2D	PCIE_85D	PCIE_TY	PCIE AP R2D C N	14 63 68
	PCIE AP D2R	PCIE_85D	PCIE_RY	PCIE AP D2R P	14 63 68
	PCIE AP D2R	PCIE_85D	PCIE_RY	PCIE AP D2R N	14 63 68
	PCIE CLK100M AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN P	63
	PCIE CLK100M AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN N	63
	PCIE CLK100M AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP P	12 63 68
	PCIE CLK100M AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP N	12 63 68
	PCIE CLK100M CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA P	12 32 68
	PCIE CLK100M CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA N	12 32 68
	PCIE CLK100M CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C P	31 32
	PCIE CLK100M CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C N	31 32
	PCIE CLK100M SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD P	12 30 68
	PCIE CLK100M SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD N	12 30 68
	PCIE CLK100M TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT P	12 23 68
	PCIE CLK100M TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT N	12 23 68
	PCIE CAMERA D2R	PCIE_85D	PCIE_RY	PCIE CAMERA D2R P	14 32 68
	PCIE CAMERA D2R	PCIE_85D	PCIE_RY	PCIE CAMERA D2R N	14 32 68
	PCIE CAMERA D2R	PCIE_85D	PCIE_RY	PCIE CAMERA D2R C P	31 32
	PCIE CAMERA D2R	PCIE_85D	PCIE_RY	PCIE CAMERA D2R C N	31 32
	PCIE CAMERA R2D	PCIE_85D	PCIE_TY	PCIE CAMERA R2D P	31 32
	PCIE CAMERA R2D	PCIE_85D	PCIE_TY	PCIE CAMERA R2D N	31 32
	PCIE CAMERA R2D	PCIE_85D	PCIE_TY	PCIE CAMERA R2D C P	14 32
	PCIE CAMERA R2D	PCIE_85D	PCIE_TY	PCIE CAMERA R2D C N	14 32

USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIA5	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?	USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIA5	*	=6X_DIELECTRIC	?	USB_RBIA5	TOP,BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?	USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?	USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?	USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5x_DIELECTRIC	?

SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?	SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?	SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?	SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET		NET TYPE		
		PHYSICAL	SPACING	
USB_BT	USB_85D	USB	USB BT P	14 29
USB_BT	USB_85D	USB	USB BT N	14 29
USB_BT	USB_85D	USB	USB BT CONN P	29 63
USB_BT	USB_85D	USB	USB BT CONN N	29 63
USB_EXTN	USB_85D	USB	USB_EXTN P	14 33
USB_EXTN	USB_85D	USB	USB_EXTN N	14 33
DEFAULT	DEFAULT	DEFAULT	SMC_DEBUGPRT_RX_L	33 36
DEFAULT	DEFAULT	DEFAULT	SMC_DEBUGPRT_TX_L	33 36
USB_EXTN	USB_85D	USB	USB2_EXTN_MUXED_P	33
USB_EXTN	USB_85D	USB	USB2_EXTN_MUXED_N	33
USB_EXTN	USB_85D	USB	USB2_EXTN_MUXED_F_P	33
USB_EXTN	USB_85D	USB	USB2_EXTN_MUXED_F_N	33
USB_EXTN	USB_85D	USB	USB_LTI1_P	68
USB_EXTN	USB_85D	USB	USB_LTI1_N	68
USB_EXTB	USB_85D	USB	USB_EXTB_P	14 63
USB_EXTB	USB_85D	USB	USB_EXTB_N	14 63
USB_TPND	USB_85D	USB	USB_TPND_P	14 34
USB_TPND	USB_85D	USB	USB_TPND_N	14 34
USB_TPND	USB_85D	USB	USB_TPND_R_P	34
USB_TPND	USB_85D	USB	USB_TPND_R_N	34
USB3_EXTN_D2R	USB_85D	USB3_RX	USB3_EXTN_D2R_P	14 33 68
USB3_EXTN_D2R	USB_85D	USB3_RX	USB3_EXTN_D2R_N	14 33 68
USB3_EXTN_R2D	USB_85D	USB3_TX	USB3_EXTN_R2D_P	33
USB3_EXTN_R2D	USB_85D	USB3_TX	USB3_EXTN_R2D_N	33 68
USB3_EXTN_R2D	USB_85D	USB3_TX	USB3_EXTN_R2D_C_P	14 33 68
USB3_EXTN_R2D	USB_85D	USB3_TX	USB3_EXTN_R2D_C_N	14 33 68
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3_EXTB_D2R_P	14 63 68
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3_EXTB_D2R_N	14 63 68
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_P	14 63 68
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_N	14 63 68
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_P	14 63 68
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_N	14 63 68
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_P	14 63
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_N	14 63
USB_NC	USB_85D	USB	NC_USB_IRP	14 66
USB_NC	USB_85D	USB	NC_USB_IRN	14 66
USB_NC	USB_85D	USB	TP_USB_5P	14
USB_NC	USB_85D	USB	TP_USB_5N	14
USB_NC	USB_85D	USB	NC_USB_SDP	14 66
USB_NC	USB_85D	USB	NC_USB_SDN	14 66
USB_NC	USB_85D	USB	NC_USB_CAMERAP	14 66
USB_NC	USB_85D	USB	NC_USB_CAMERAN	14 66
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	14
SATA_85D	SATA_85D	SATA_RX	DUMMY_SATA_D2R_P	
SATA_85D	SATA_85D	SATA_RX	DUMMY_SATA_D2R_N	
SATA_85D	SATA_TX	SATA_TX	DUMMY_SATA_R2D_P	
SATA_85D	SATA_TX	SATA_TX	DUMMY_SATA_R2D_N	
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	31 32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	32
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 23
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	23

Notes:
This is here to keep the SATA rules.

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SYNC DATE=08/12/2013

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USB Constraints

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	= 2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	= 2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD







































































SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?


PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

PCH Net Properties

ELECTRICAL CONST SET		NET TYPE			
	PHYSICAL		SPACING		
	LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 36 45 68
	LPC_AD	LPC_45S	LPC	LPC_FRAME_L	14 36 45 68
	LPC_CLK24M_SMC	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
	LPC_CLK24M_SMT	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 36 68
	LPC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	17 45 68
	LPC_CLK24M_LPCPLUS	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R	12 17
	SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_CLK	14 16 19 39 63 68
	SMBUS_PCH	SMB_45S	SMB	SMBUS_PCH_DATA	14 16 19 39 63 68
	SMT_PCH_0	SMB_45S	SMB	SML_PCH_0_CLK	14 39
	SMT_PCH_0	SMB_45S	SMB	SML_PCH_0_DATA	14 39
		SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	14 32 36 39 43 68 76
		SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	14 32 36 39 43 68 76
	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 47
	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK_R	12
	HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 47
	HDA_SYNC	HDA_45S	HDA	HDA_SYNC_R	12
	HDA_RST	HDA_45S	HDA	HDA_RST_R_L	12
	HDA_RST	HDA_45S	HDA	HDA_RST_L	12 47
	HDA_SDIN	HDA_45S	HDA	HDA_SDIN0	12 47 68
	HDA_SDIN	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	47
	HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 47
	HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT_R	12 17
	SPT_MLB	SPT_45S	SPT	SPI_ALT_CLK	45
	SPT_MLB	SPT_45S	SPT	SPI_CLK	45
	SPT_MLB	SPT_45S	SPT	SPI_CLK_R	14 45
	SPT_MLB	SPT_45S	SPT	SPI_MLB_CLK	45
	SPT_MLB	SPT_45S	SPT	SPI_SMC_CLK	36 45
	SPT_MLB	SPT_45S	SPT	SPI_ALT_CS_L	45
	SPT_MLB	SPT_45S	SPT	SPI_CS0_L	45
	SPT_MLB	SPT_45S	SPT	SPI_CS0_R_L	14 45
	SPT_MLB	SPT_45S	SPT	SPI_MLB_CS_L	45
	SPT_MLB	SPT_45S	SPT	SPI_SMC_CS_L	36 45
	SPT_MLB	SPT_45S	SPT	SPI_ALT_MISO	45
	SPT_MLB	SPT_45S	SPT	SPI_MISO	14 45
	SPT_MLB	SPT_45S	SPT	SPI_MISO_R	45
	SPT_MLB	SPT_45S	SPT	SPI_MLB_MISO	45
	SPT_MLB	SPT_45S	SPT	SPI_SMC_MISO	36 45
	SPT_MLB	SPT_45S	SPT	SPI_ALT_MOSI	45
	SPT_MLB	SPT_45S	SPT	SPI_MOSI	45
	SPT_MLB	SPT_45S	SPT	SPI_MOSI_R	14 45
	SPT_MLB	SPT_45S	SPT	SPI_MLB_MOSI	45
	SPT_MLB	SPT_45S	SPT	SPI_SMC_MOSI	36 45
	SPT_MLB_IO2	SPT_45S	SPT	SPI_IO<2>	14 45
	SPT_MLB_IO2	SPT_45S	SPT	SPIROM_WP_L	45
	SPT_MLB_IO3	SPT_45S	SPT	SPI_IO<3>	14 45
	SPT_MLB_IO3	SPT_45S	SPT	SPIROM_HOLD_L	45
	SPT_MLB_IO3	SPT_45S	SPT	SPIROM_USE_MLB	15 45 68
	PCH_RTCX	PCH_45S	PCH_15MTL	PCH_CLK32K_RTCX1	12 17
	PCH_SRTCST	PCH_45S	PCH_15MTL	PCH_SRTCST_L	12
	PCH_RTCRST	PCH_45S	PCH_15MTL	RTC RESET_L	12
	PCH_THRMTRIP	PCH_45S	PCH_18MTL	PM_THRMTRIP_L	16 37
	PCH_THRMTRIP	PCH_45S	PCH_18MTL	PM_THRMTRIP_R_L	37
		PCH_45S	PCH_15MTL	PCH_INTRUDER_L	12
		PCH_45S	PCH_15MTL	PCH_INTVRMEN	12
		PCH_45S	PCH_15MTL	PCH_DSWVRMEN	13
		PCH_45S	PCH_15MTL	PM_RSMRST_L	13 61
		PCH_45S	PCH_15MTL	PM_SYSRST_L	13 17 36 68
		PCH_45S	PCH_15MTL	XDP_DBRESET_L	16 17
		PCH_45S	PCH_15MTL	PM_PCH_SYS_PWROK	13 16 17 36
		PCH_45S	PCH_15MTL	XDP_SYS_PWROK	16
		PCH_45S	PCH_15MTL	SYS_PWROK_R	17
		PCH_45S	PCH_15MTL	PM_PCH_PWROK	13 17
		PCH_45S	PCH_15MTL	PM_S0_PGOOD	17
		PCH_45S	PCH_15MTL	PMC_DELAYED_PWRGD	17 24 25 36 37
		PCH_45S	PCH_15MTL	PM_DSW_PWRGD	13 36
		PCH_45S	PCH_15MTL	PM_PWRBTN_L	13 16 36
		PCH_45S	PCH_15MTL	XDP_CPU_PWRBTN_L	16
		PCH_45S	PCH_15MTL	PCIE_WAKE_L	13 29 31
		PCH_45S	PCH_15MTL	AP_PCIE_WAKE_L	29 63
		PCH_45S	PCH_15MTL	CAM_PCIE_WAKE_L	31
		PCH_45S	PCH_15MTL	TBT_CIO_PLUGIN_EVENT_L	15 18 23
	PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALIN	12 17
	PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALOUT	12 17
	PCH_CLK24M_XTAL	PCH_45S	PCH_20MTL	PCH_CLK24M_XTALOUT_R	17
	PCH_RCOMP_PCIE	PCH_27P4S	PCH_12MTL	PCH_PCIE_RCOMP	14
	PCH_RCOMP_OBT	PCH_27P4S	PCH_12MTL	PCH_OPI_COMP	15
	PCH_RCOMP_SATA	PCH_27P4S	PCH_12MTL	PCH_SATA_RCOMP	12

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONST SET		NET TYPE		
		PHYSICAL	SPACING	
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK P 31 32
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM CAM CLK N 31 32
	S2_MEM_CKE	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CKE 31 32
	S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CS L 31 32
	S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM CAM ODT 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM CAS L 31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM CAM RAS L 31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM WE L 31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<0> 31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<1> 31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM CAM BA<2> 31 32
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS P<0> 31 32
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM CAM DQS N<0> 31 32
	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS P<1> 31 32
	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM CAM DQS N<1> 31 32
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DM<0> 31 32
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DM<1> 31 32
	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM CAM A<14..0> 31 32
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM CAM DQ<7..0> 31 32
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM CAM DQ<15..8> 31 32
	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA P 31 32 68
	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA N 31 32 68
	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN P 32 68
	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI DATA CONN N 32 68
	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK P 31 32 68
	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK N 31 32 68
	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN P 32 68
	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI CLK CONN N 32 68
		S2_MEM_PWR		PP1V35_CAM 31 32
		S2_MEM_PWR		PP0V675_CAM_VREF 31 32
		S2_MEM_PWR		PP0V675_MEM_CAM_VREFCA 32
		S2_MEM_PWR		PP0V675_MEM_CAM_VREFDO 32

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=1TO1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=1TO1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.070 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.100 MM	500 MIL		
CPU_27P4S	BOTTOM			0.230 MM	100 MIL		
USB3_85D	TOP			0.100 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DDR3 Loaded Segment Constraint Relaxations

Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_MEM	MEM_45S
MEM_72D	BGA_MEM	MEM_85D

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.100 MM	6.35 MM		

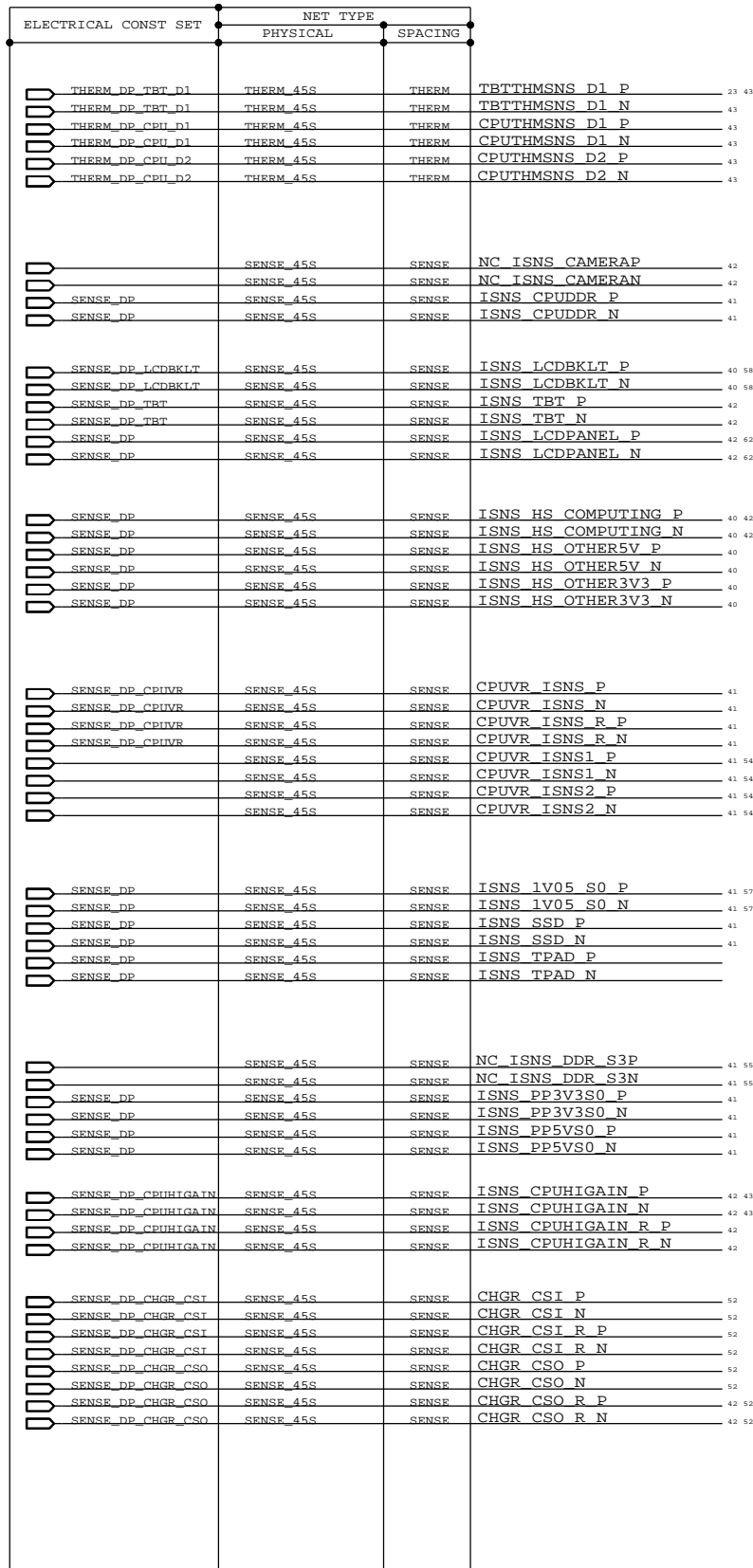
DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

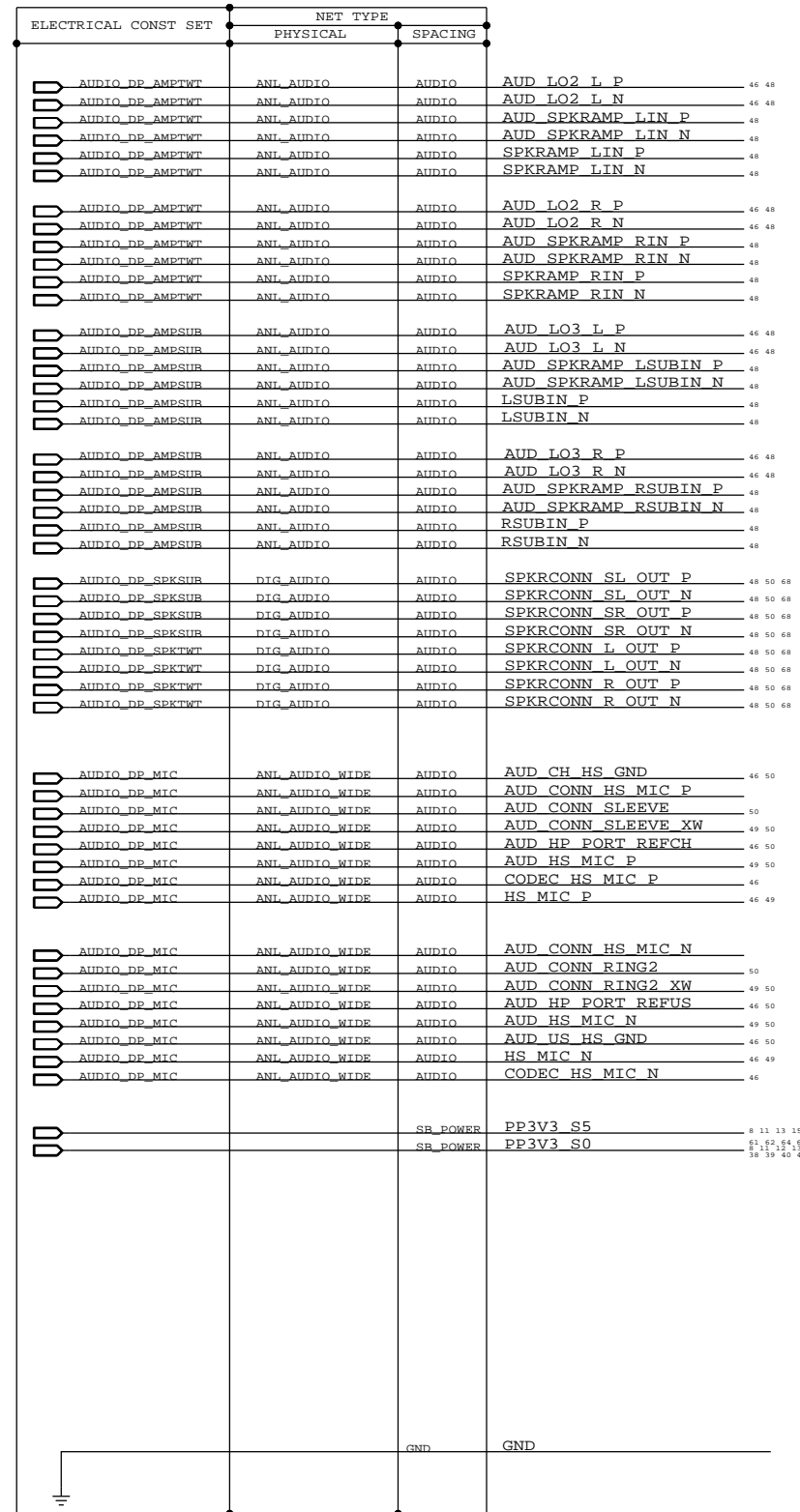
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA


NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO
1T01_DIFFPAIR	*	1T01_DIFFPAIR

J44 Specific Net Properties



J44 Specific Net Properties



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